

FIG. 1A

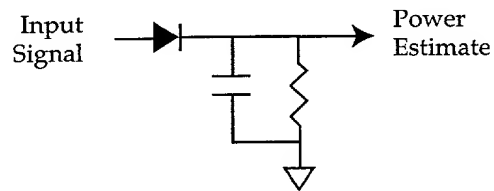


FIG. 1B

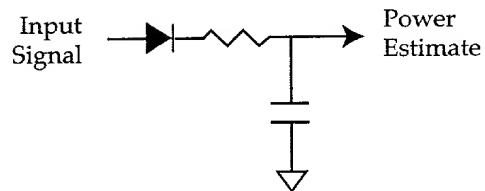


FIG. 1C

000001 51222250

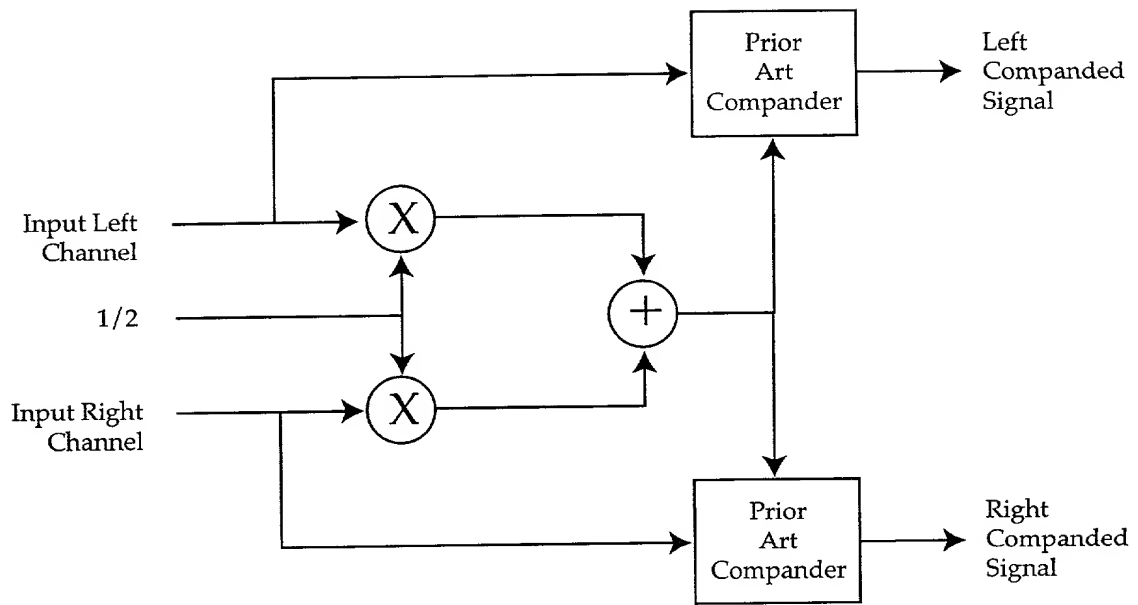


FIG. 1D

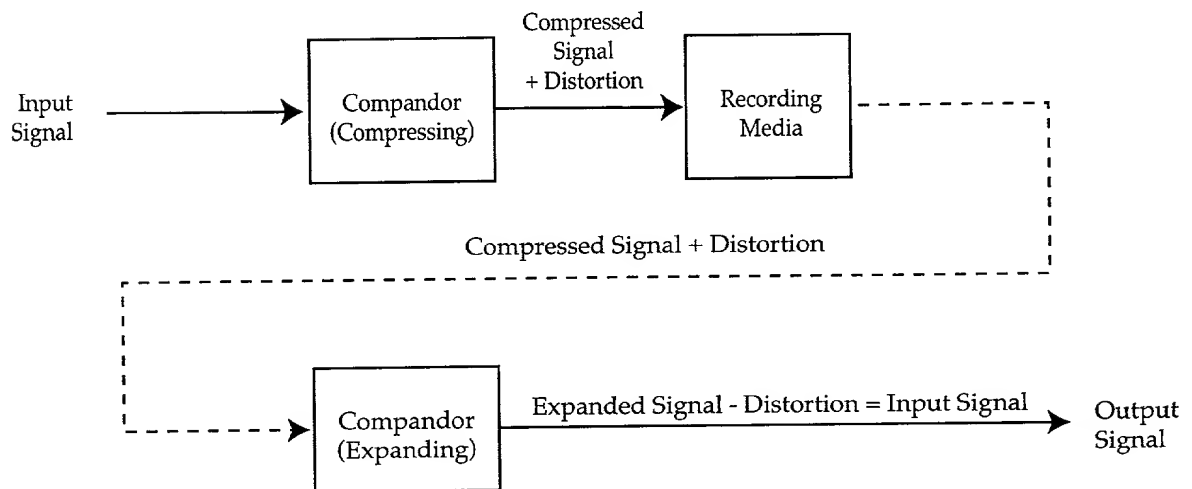


FIG. 1E

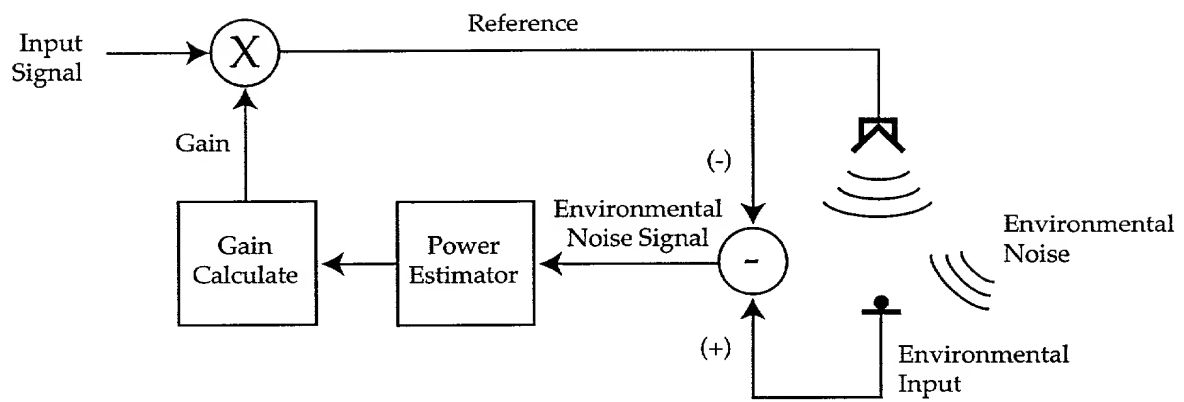


FIG. 2

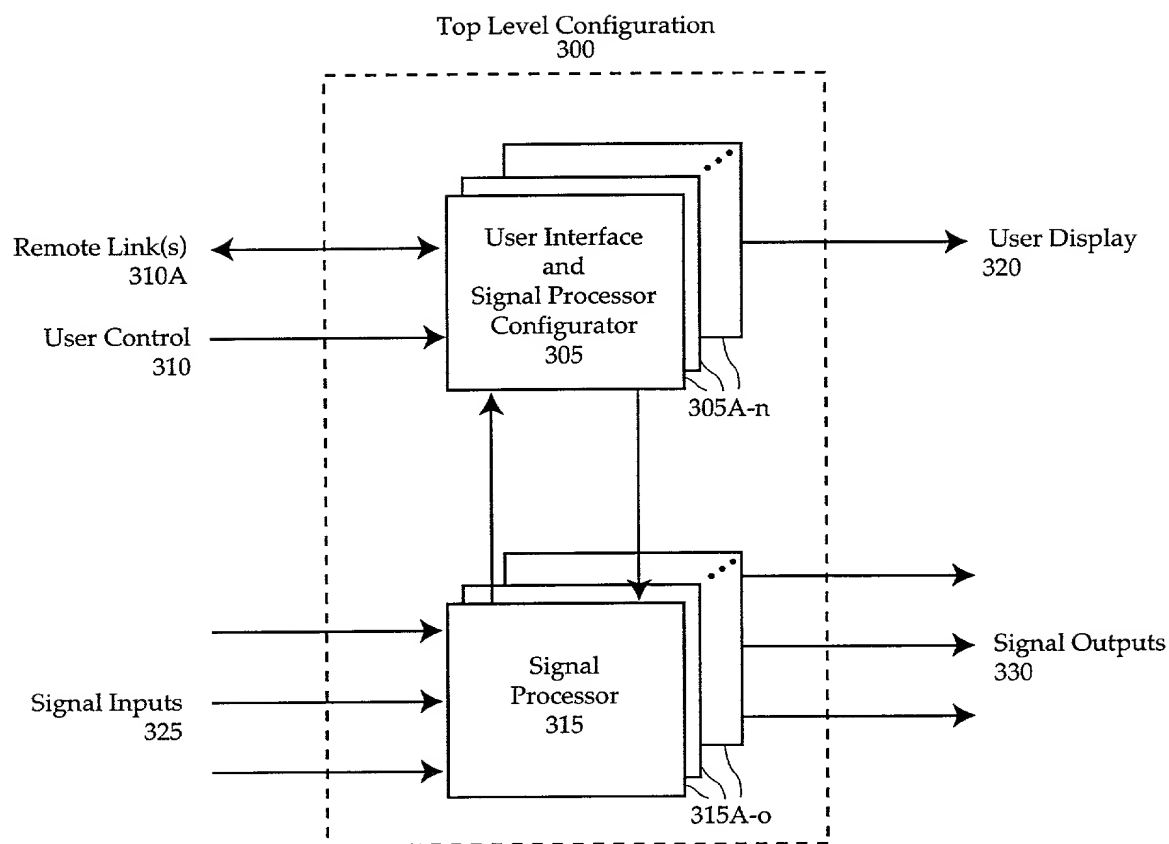


FIG. 3A

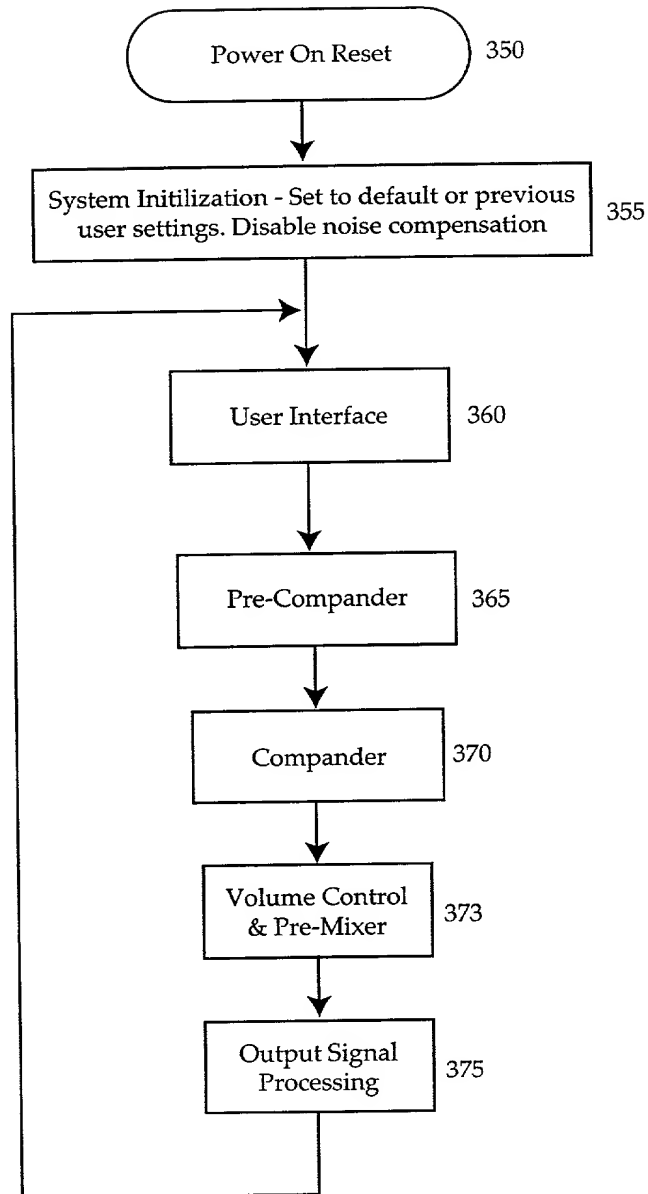


FIG. 3B

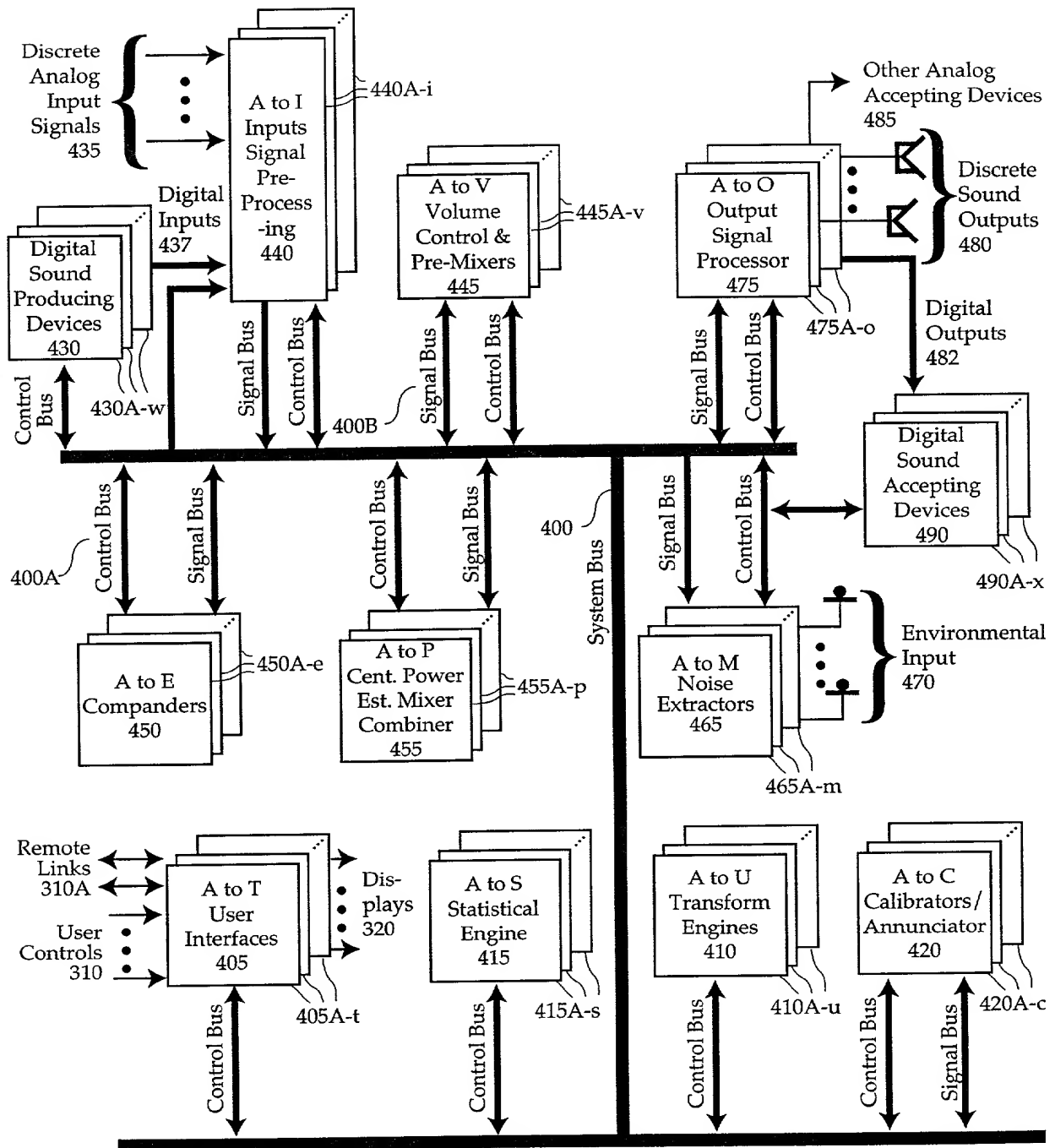


FIG. 4

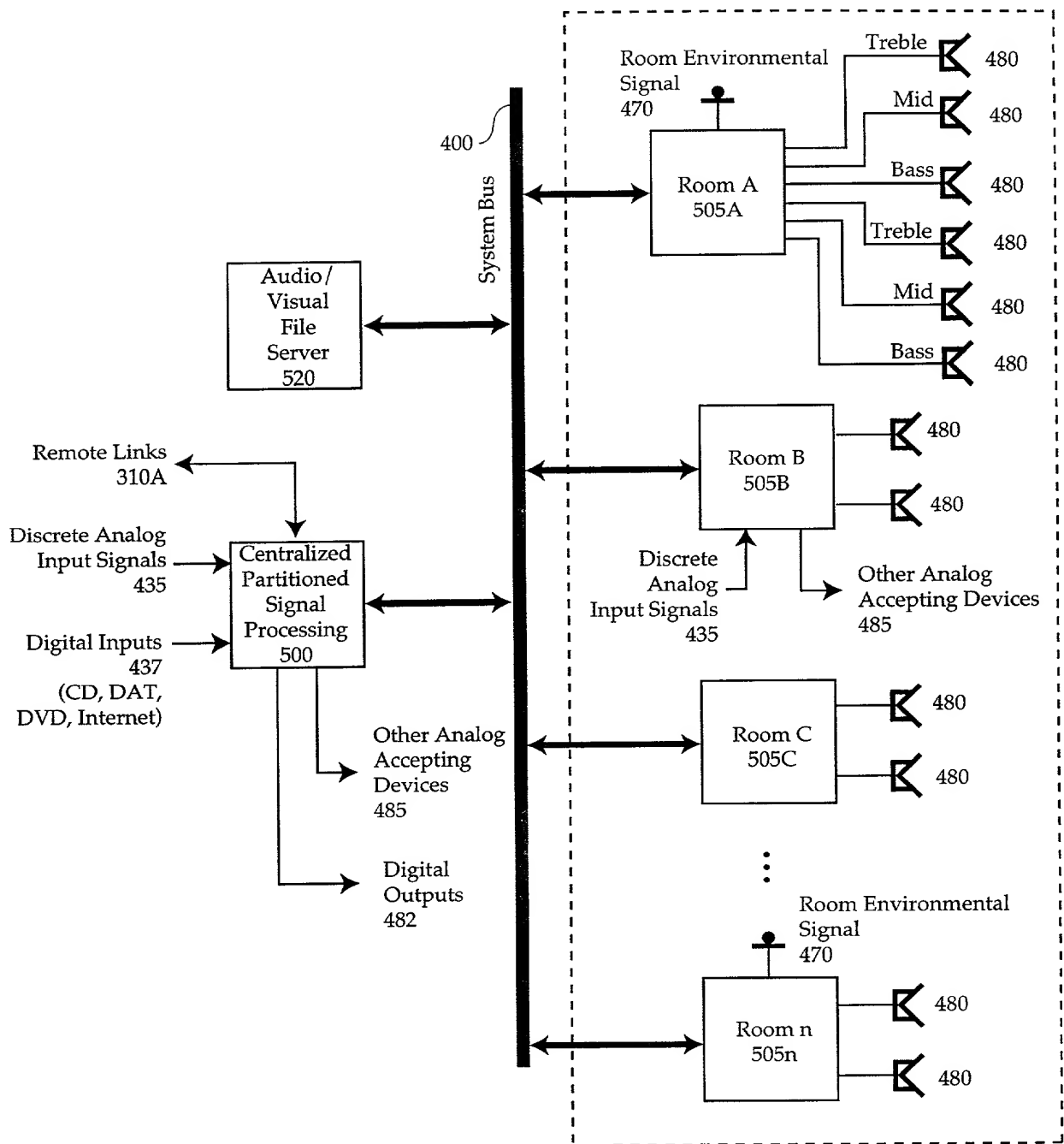


FIG. 5A

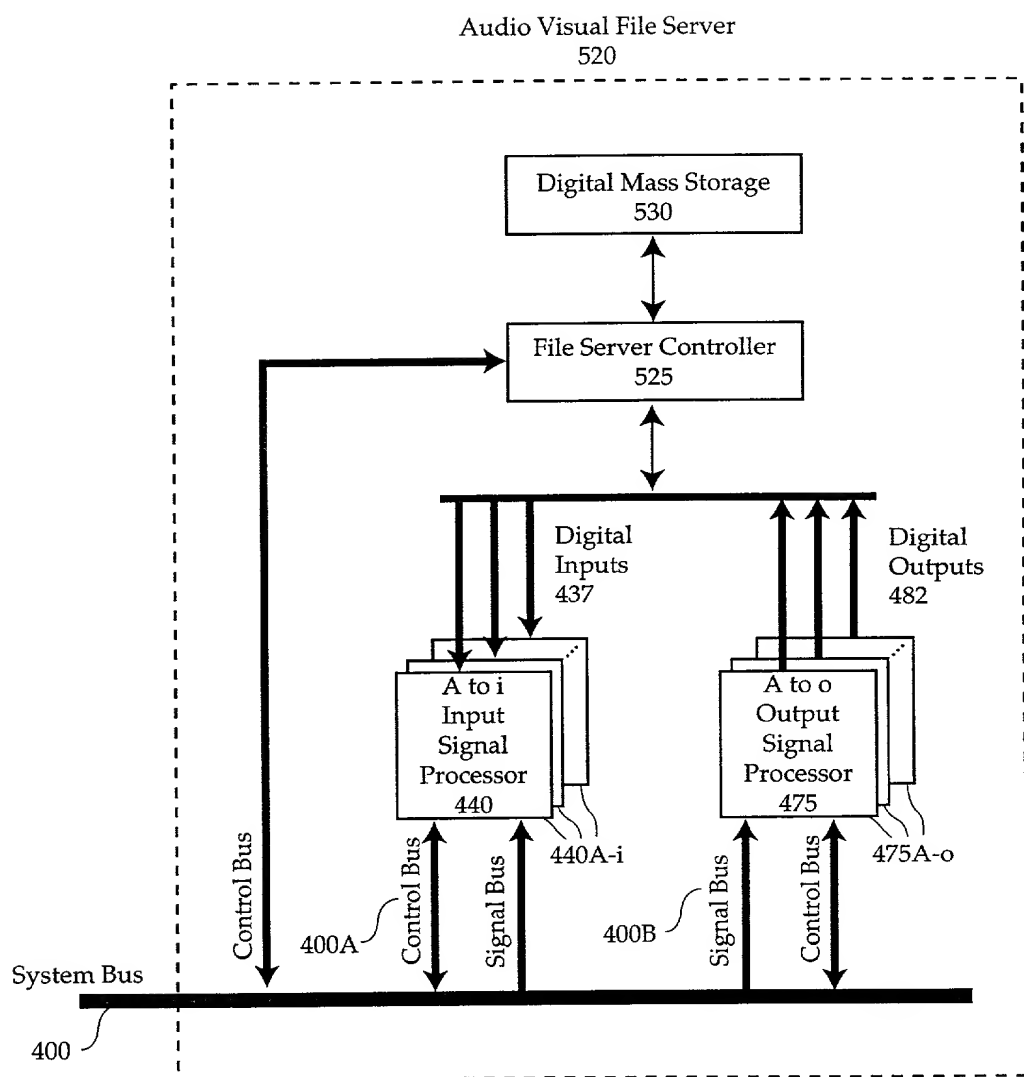


FIG. 5B

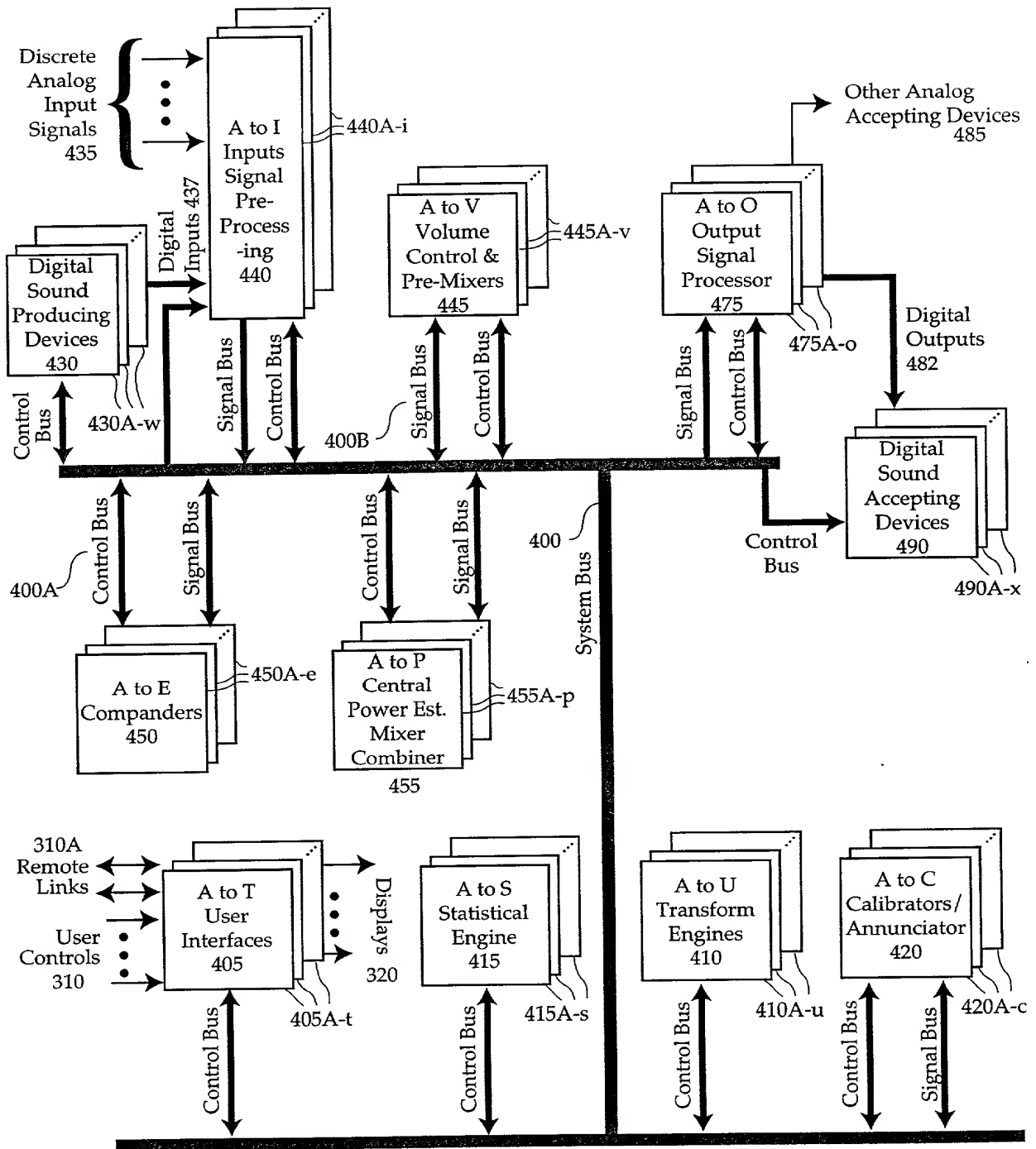


FIG. 5C

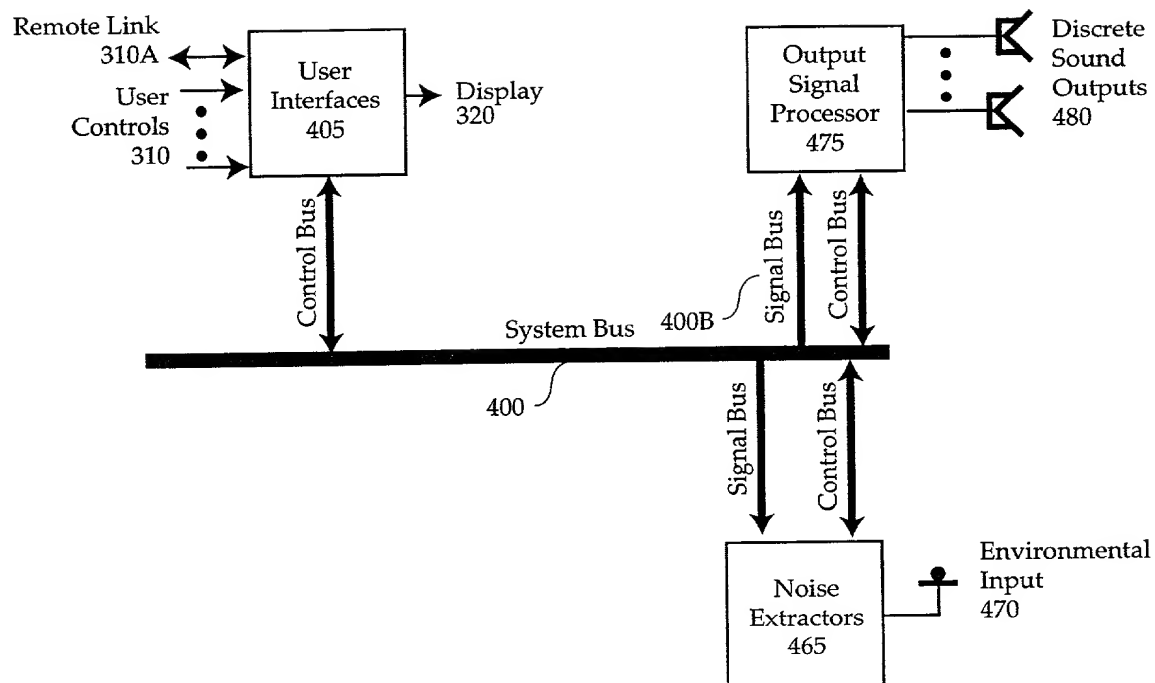


FIG. 5D

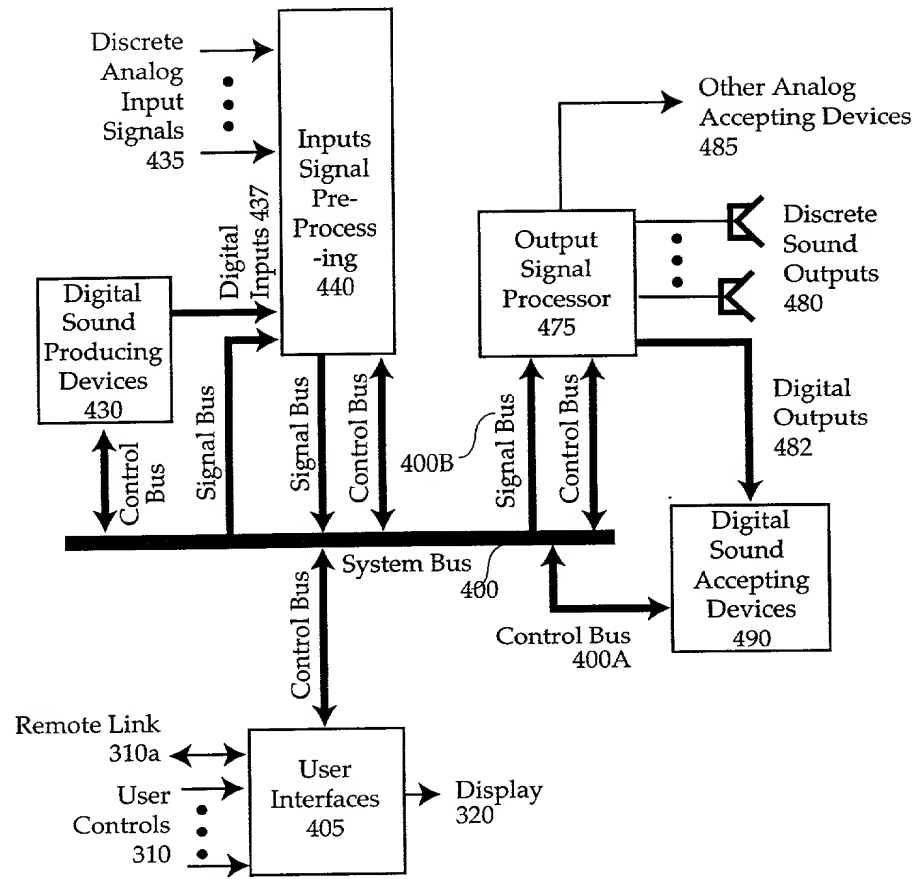


FIG. 5E

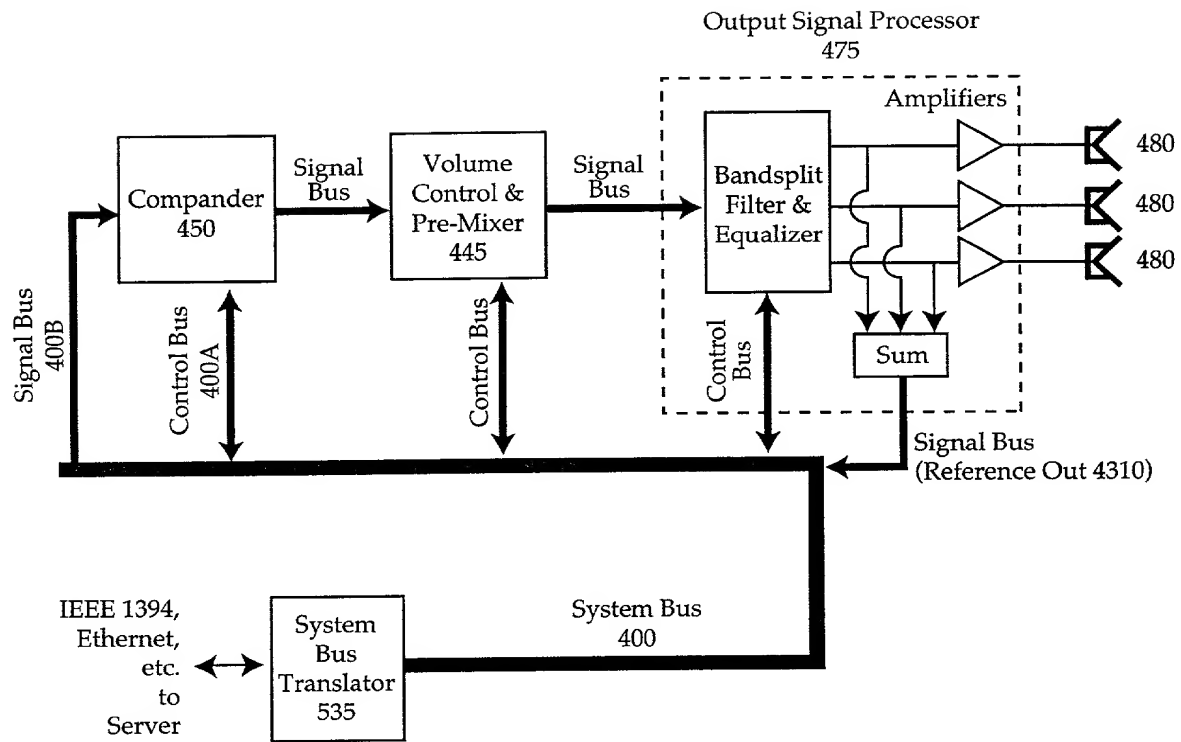


FIG. 5F

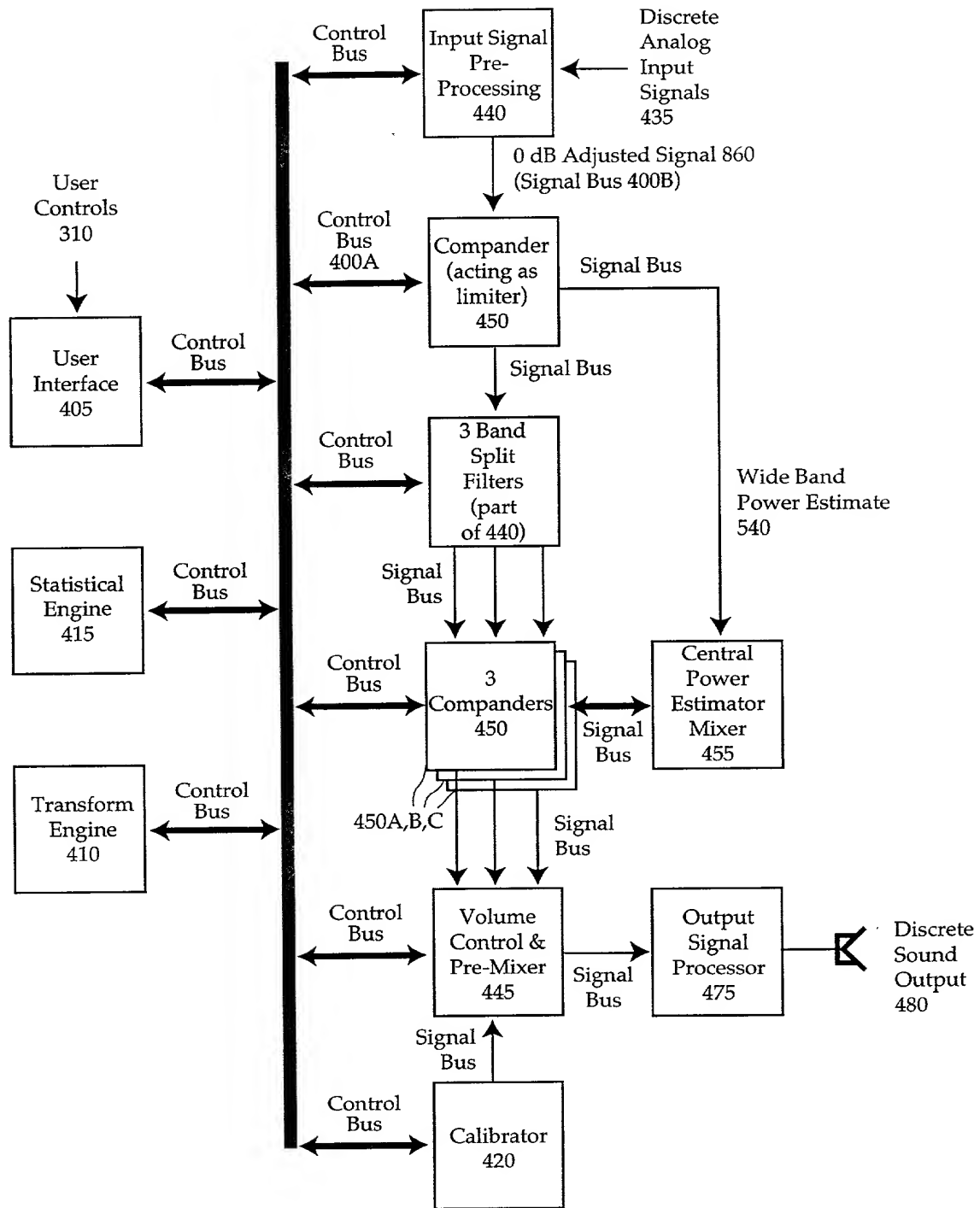


FIG. 5G

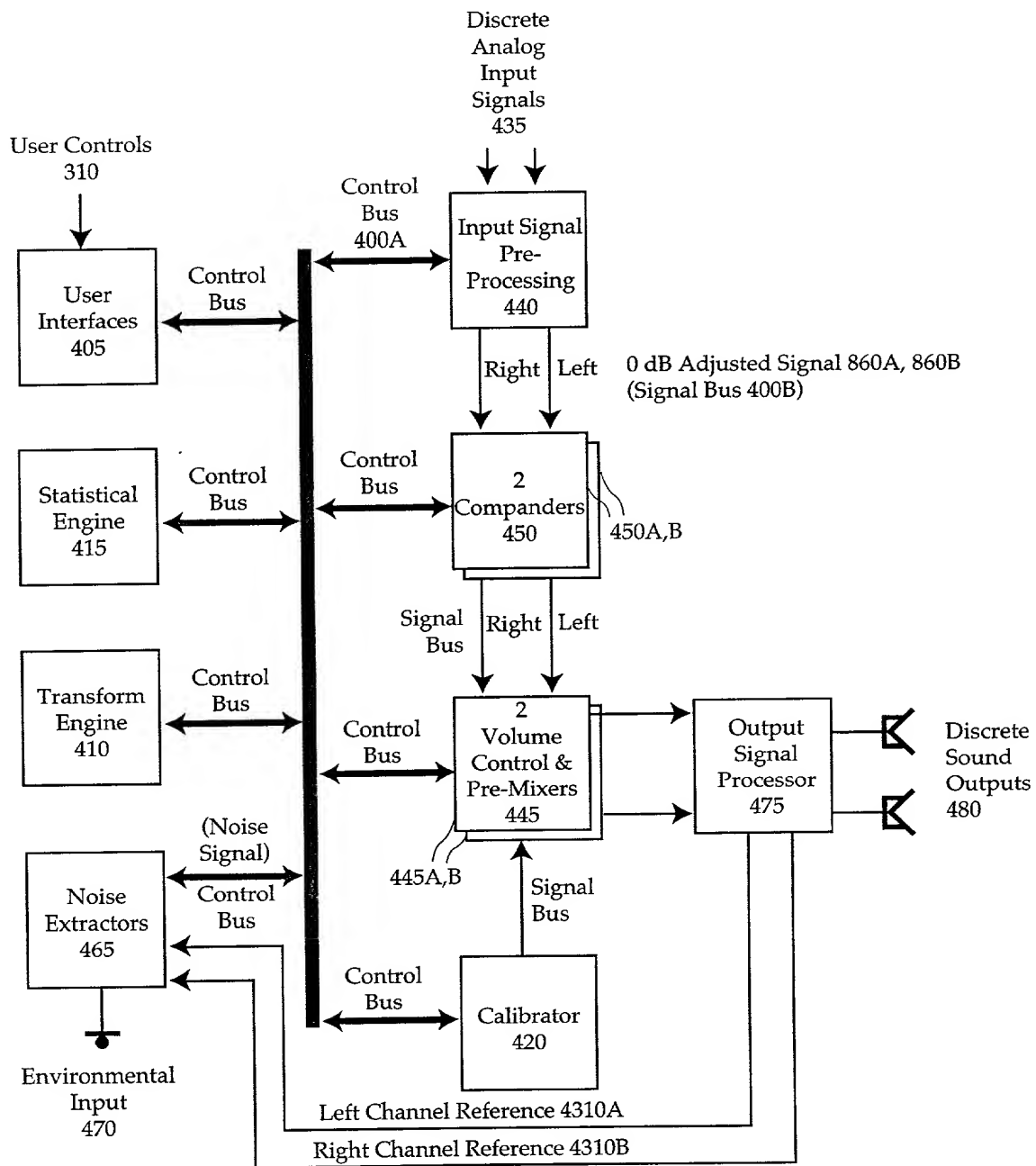


FIG. 5H

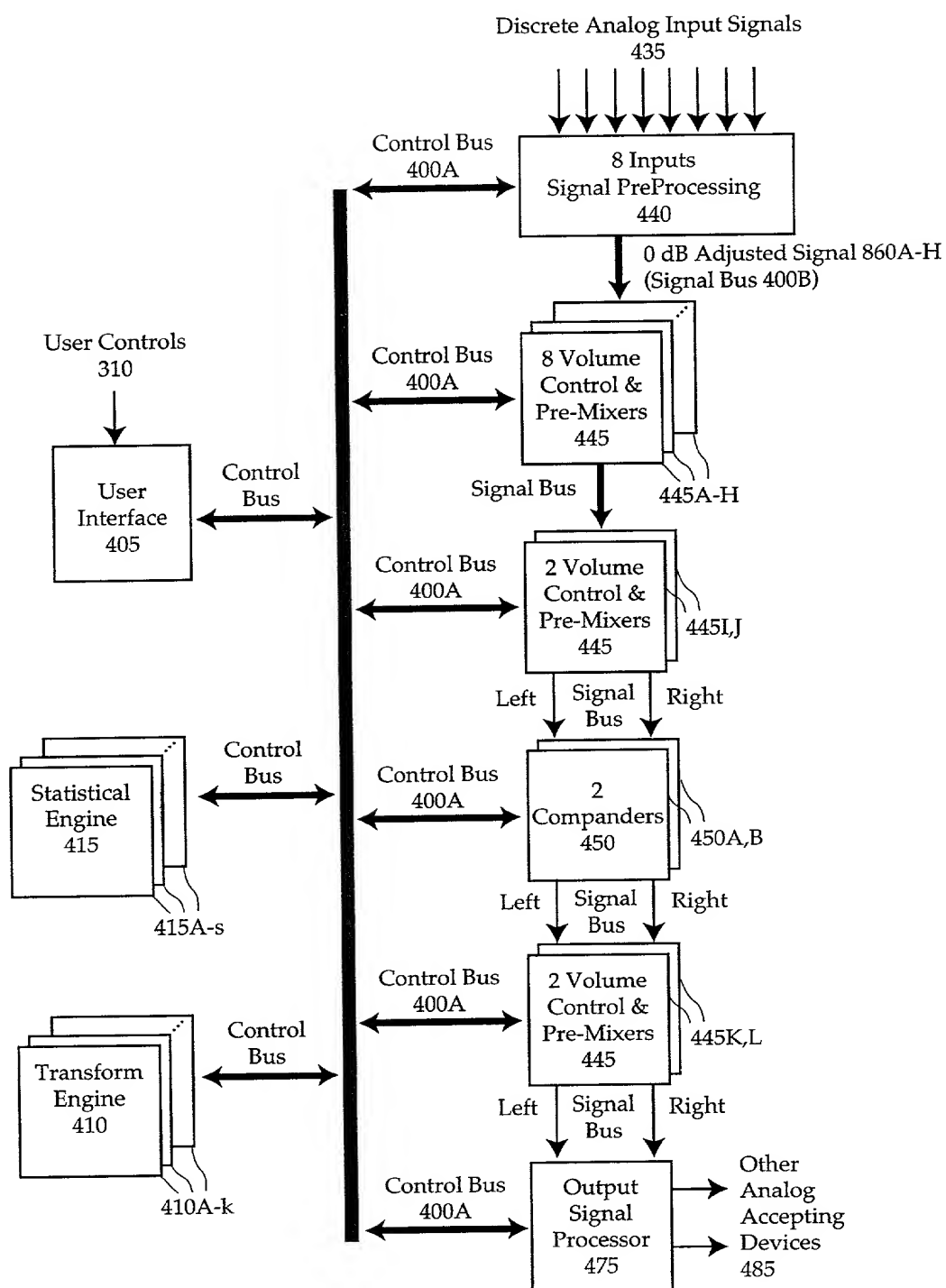


FIG. 5I

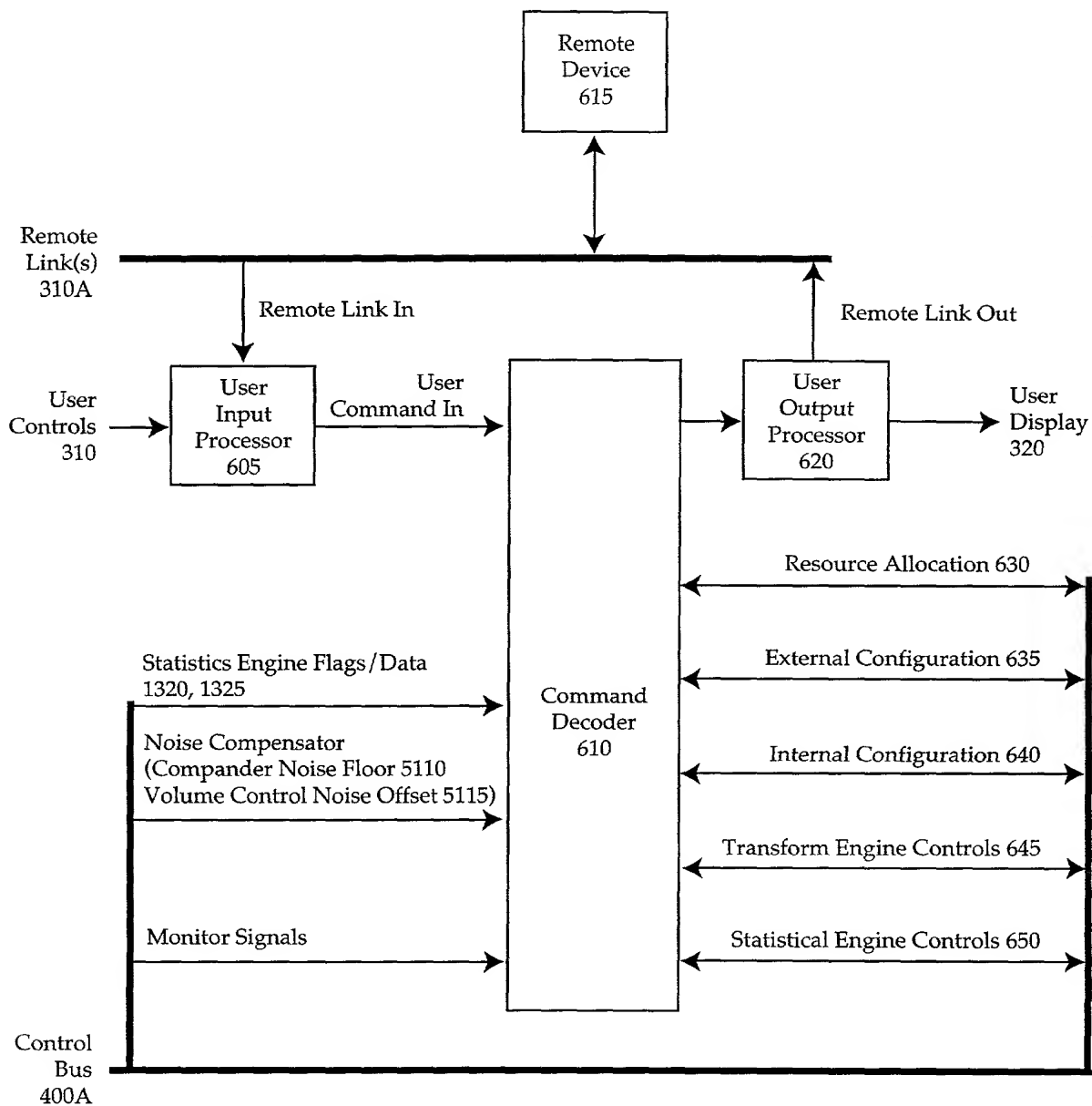


FIG. 6A

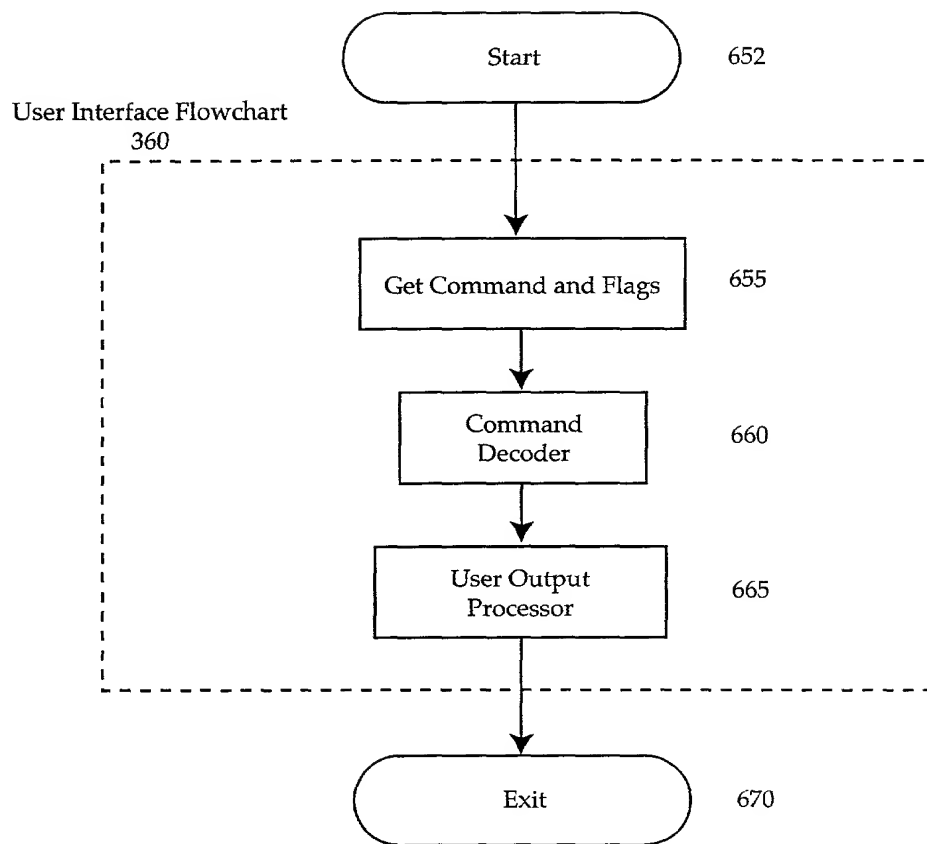


FIG. 6B

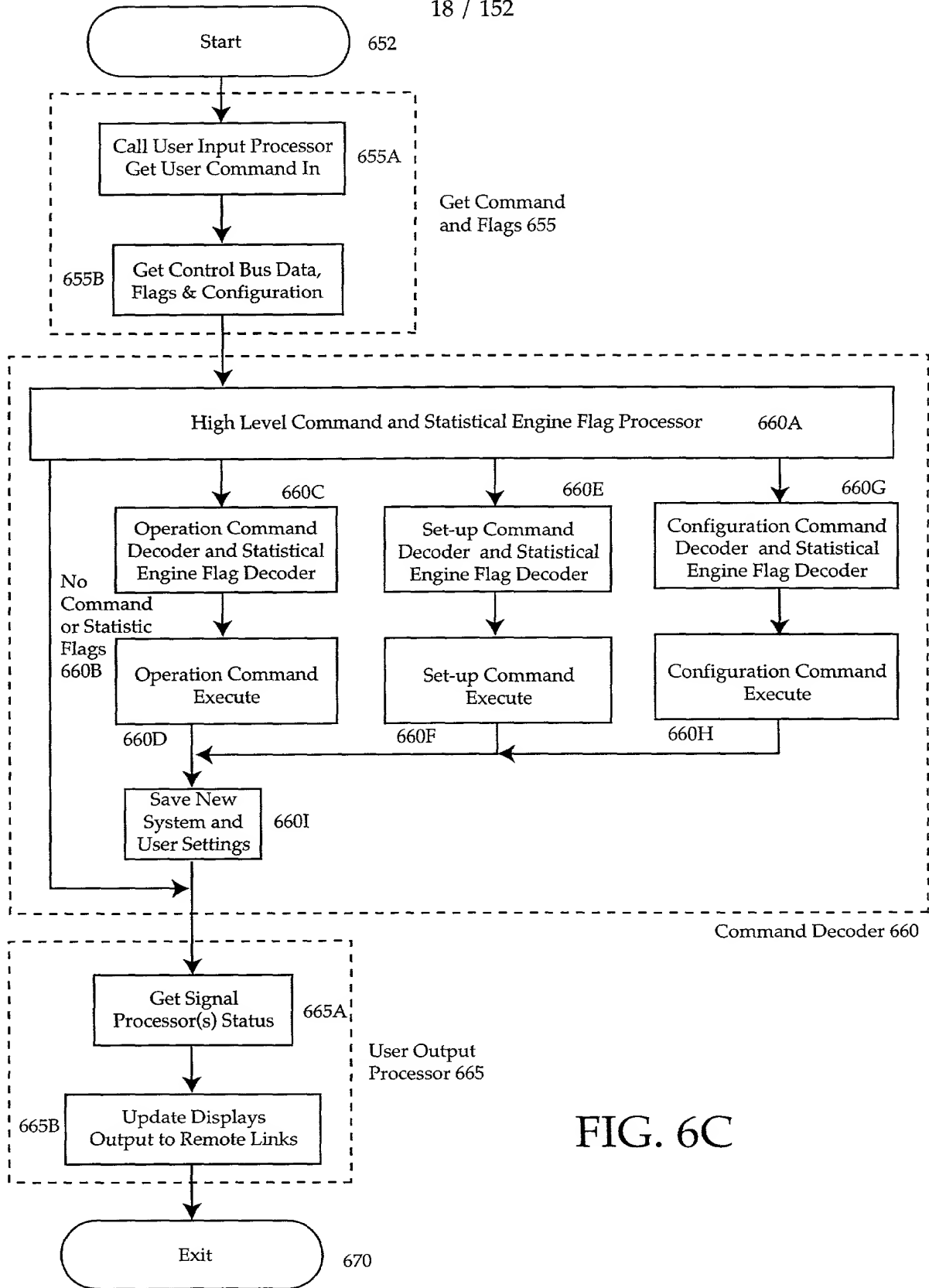


FIG. 6C

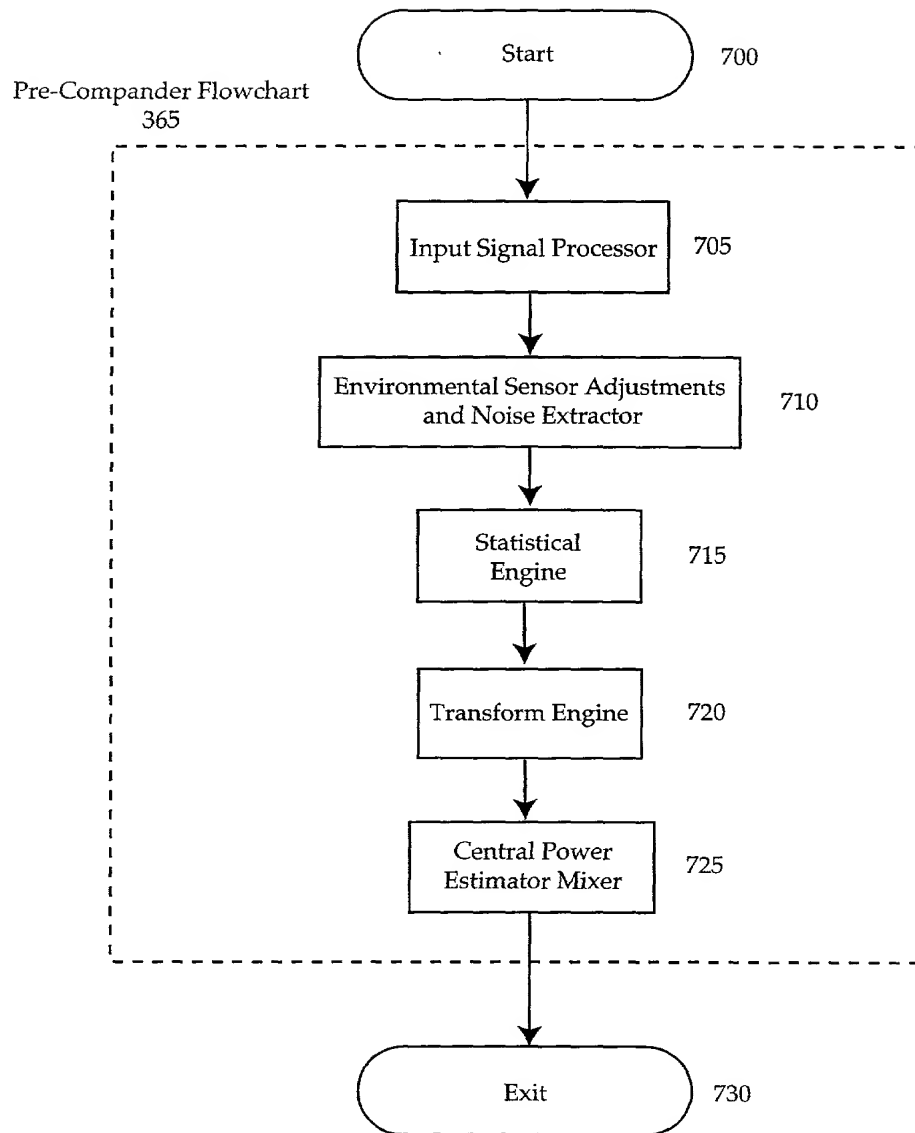


FIG. 7

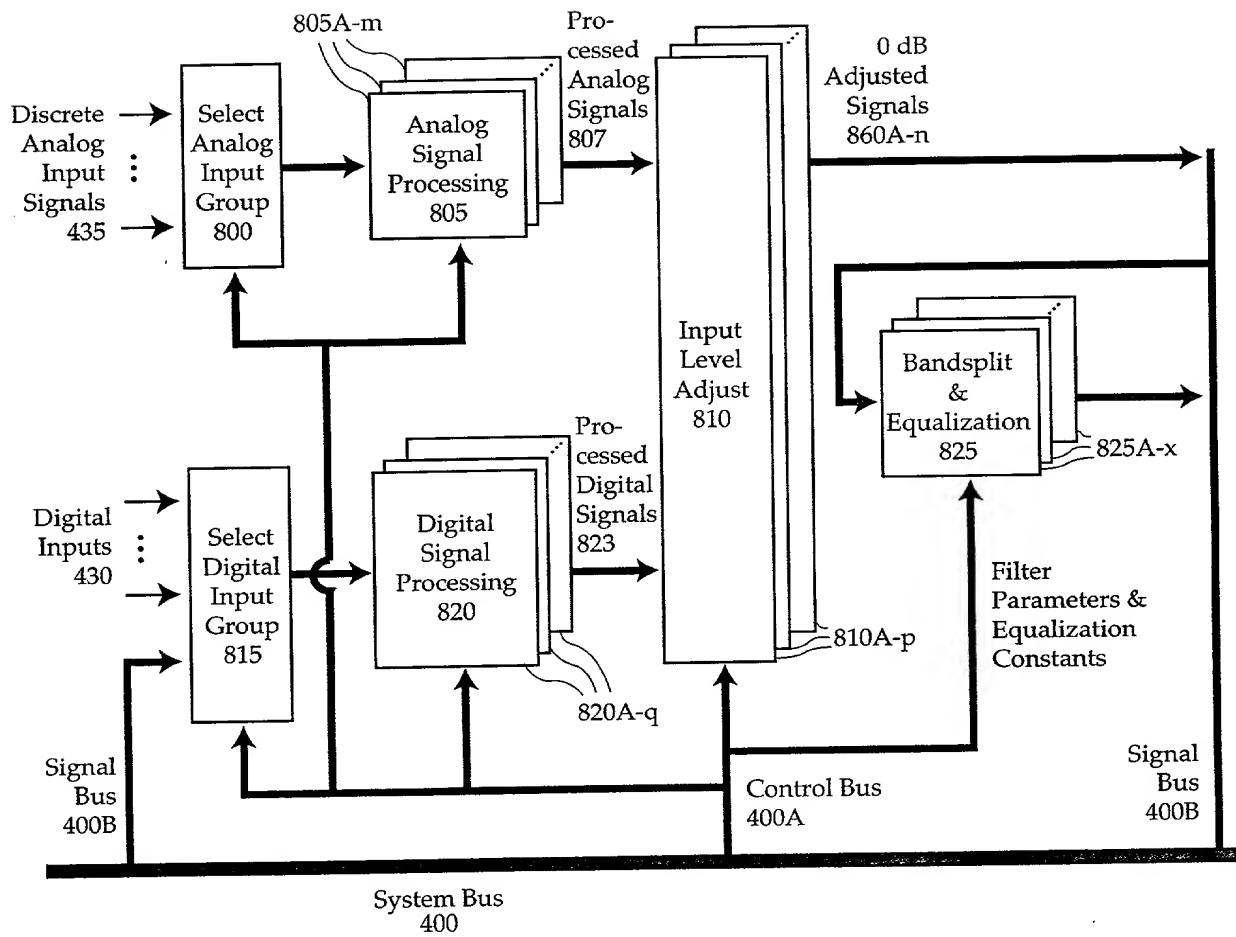


FIG. 8A

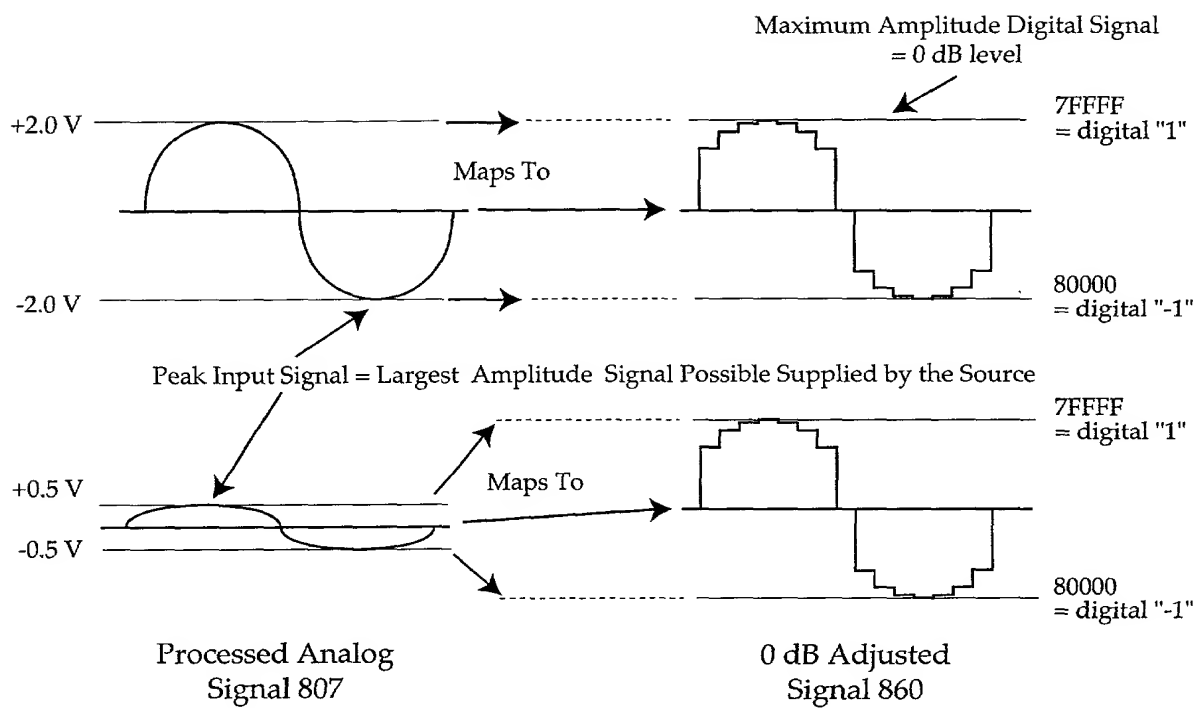


FIG. 8B

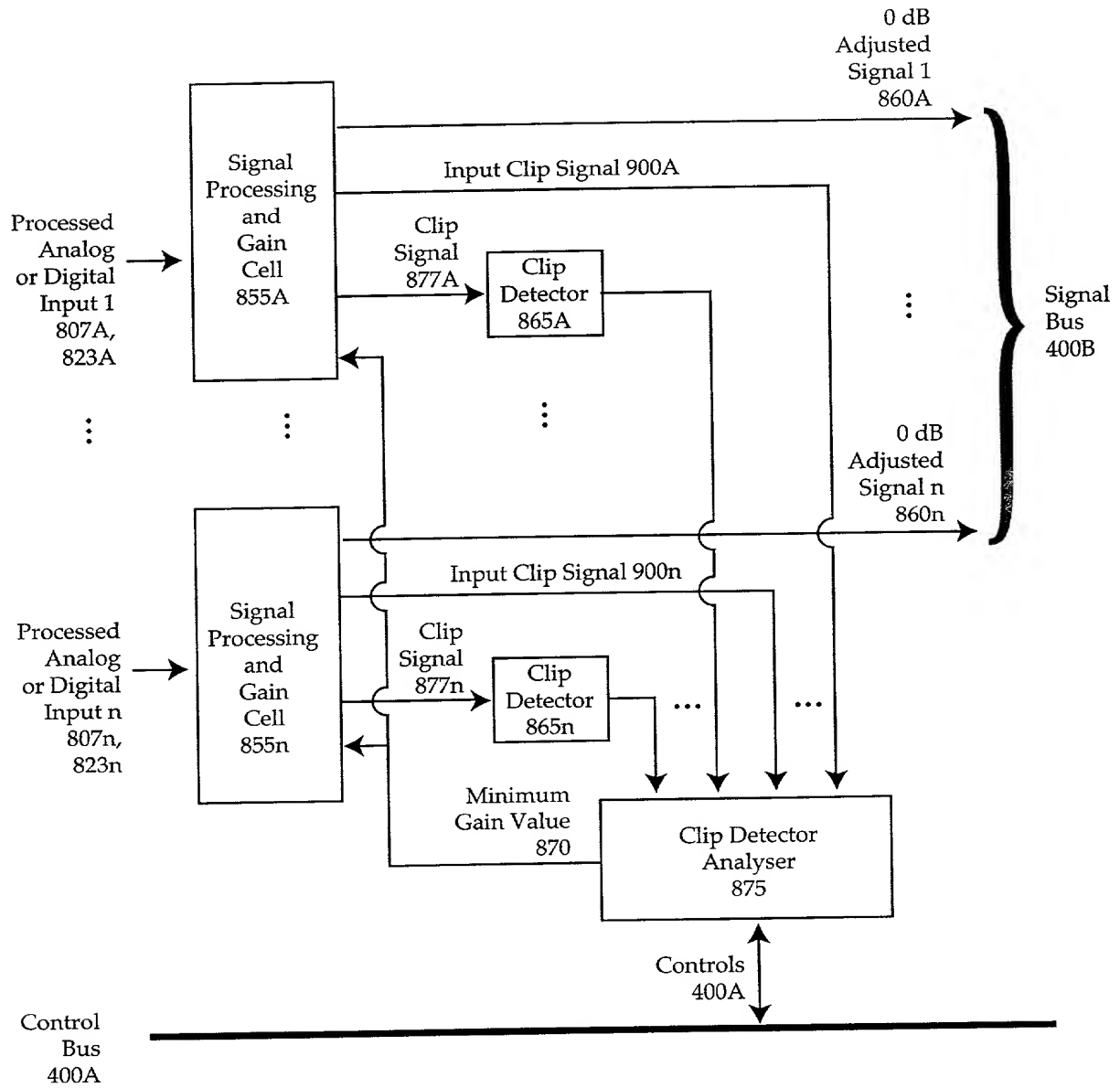


FIG. 8C

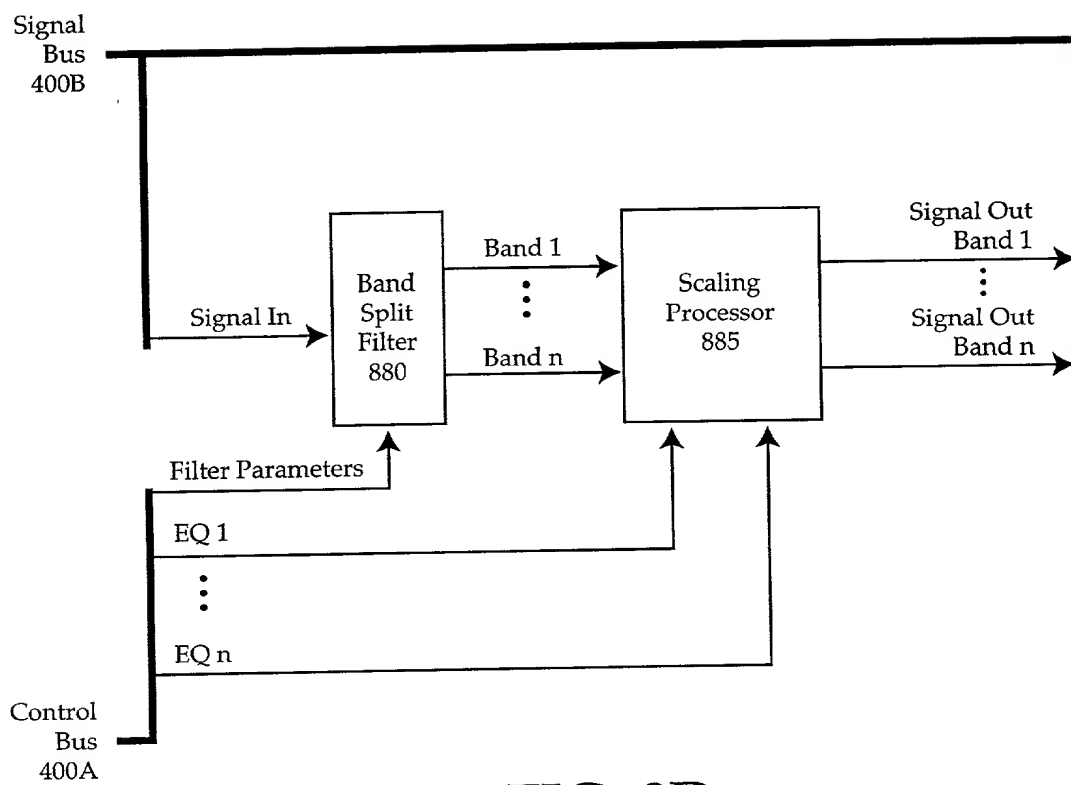


FIG. 8D

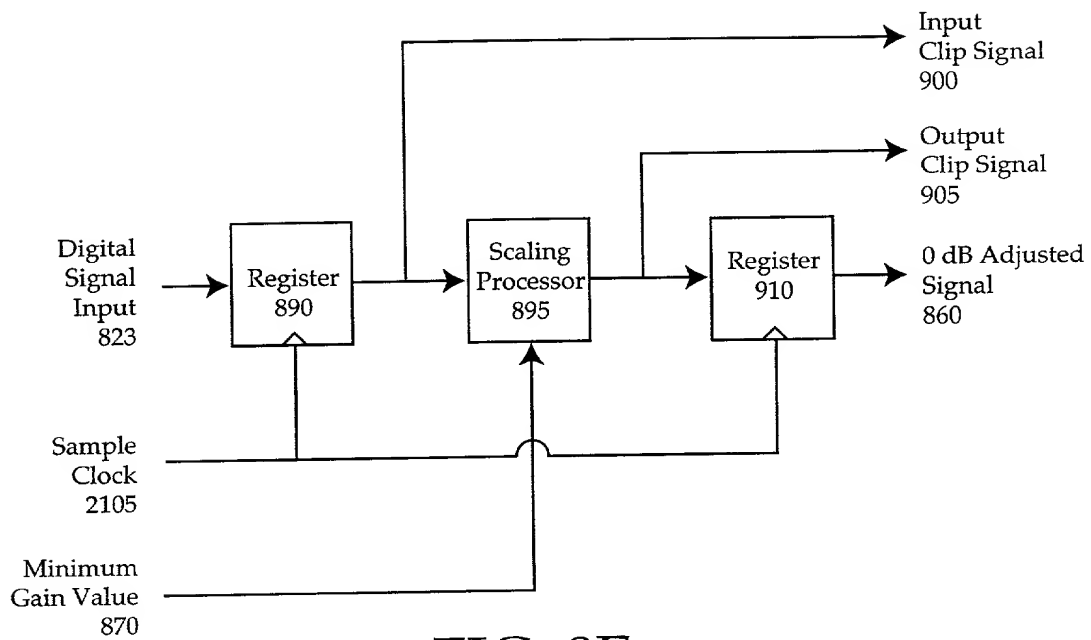


FIG. 8E

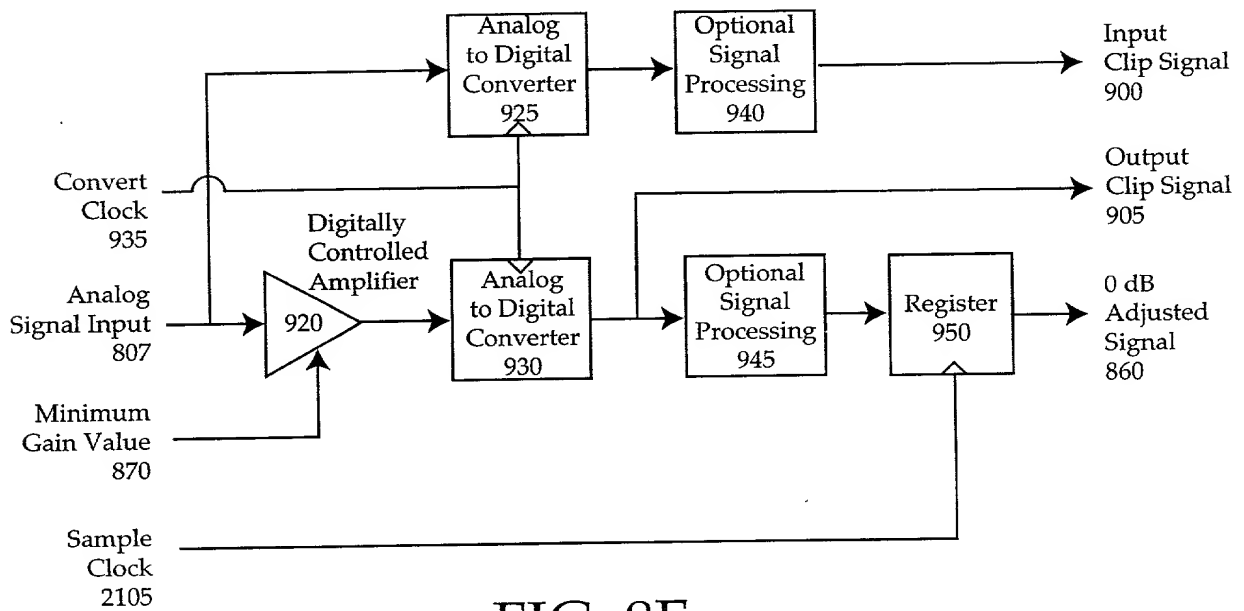


FIG. 8F

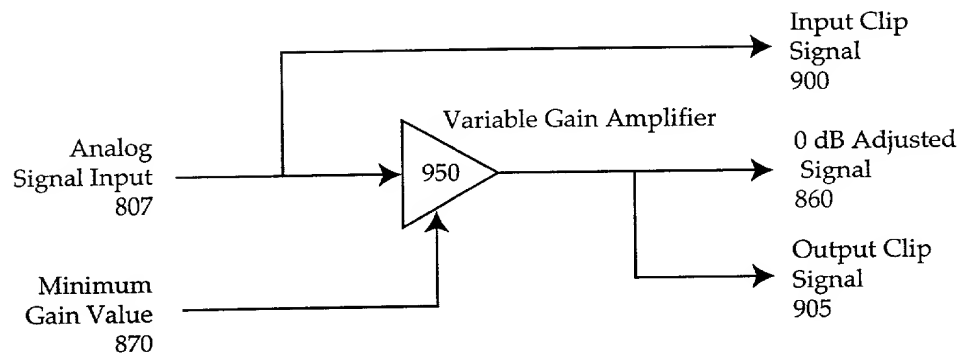


FIG. 8G

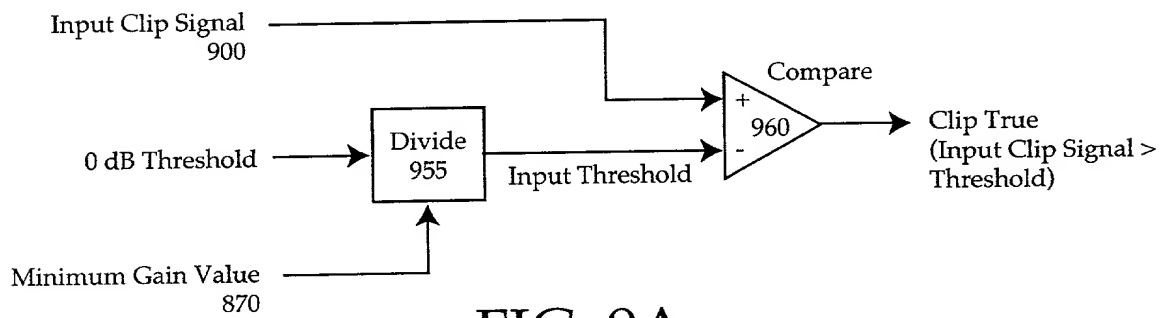


FIG. 9A

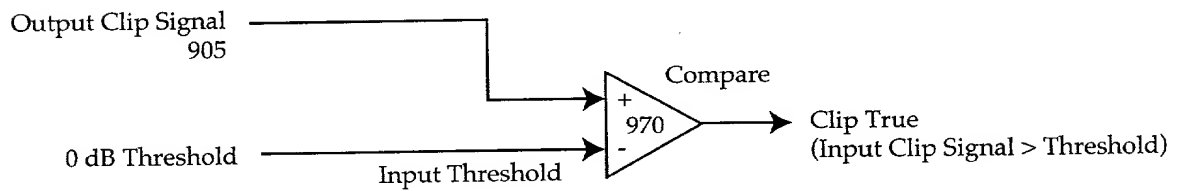


FIG. 9B

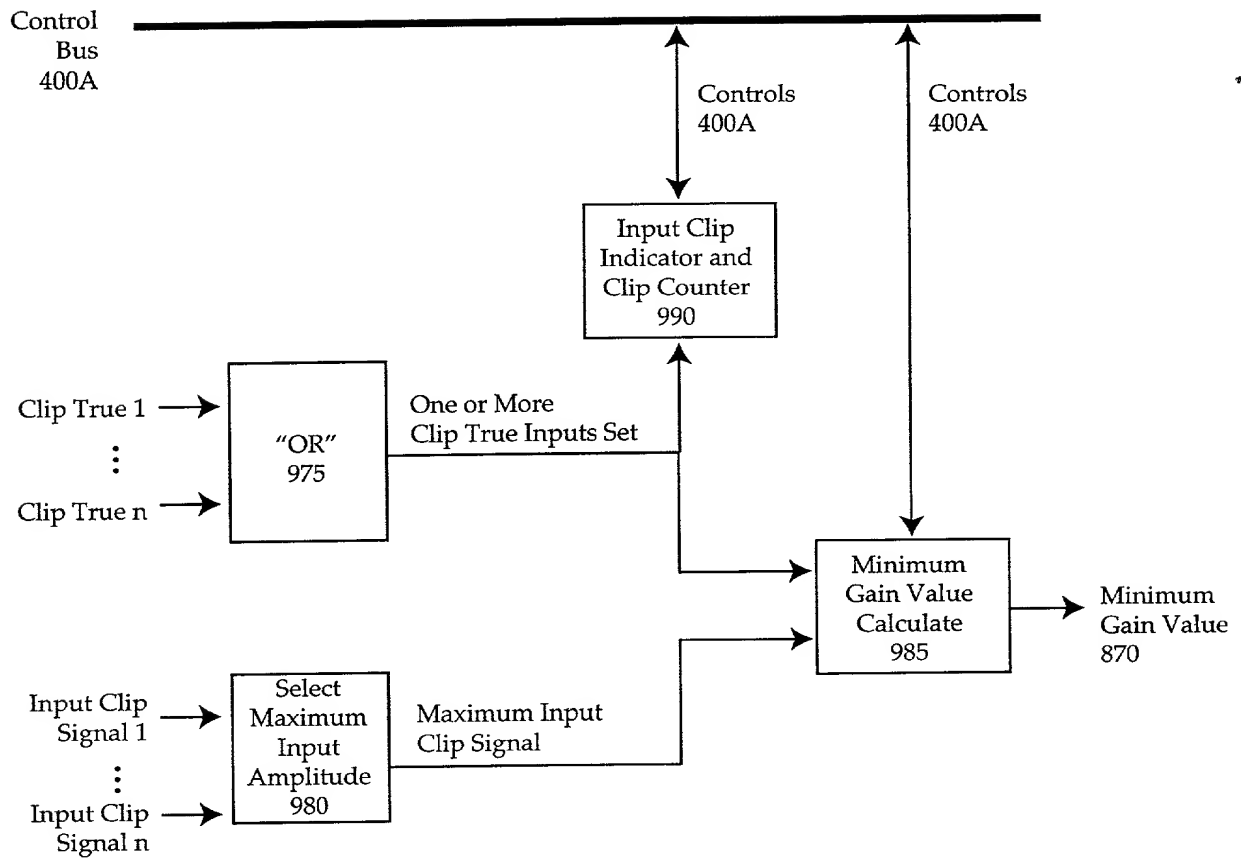


FIG. 9C

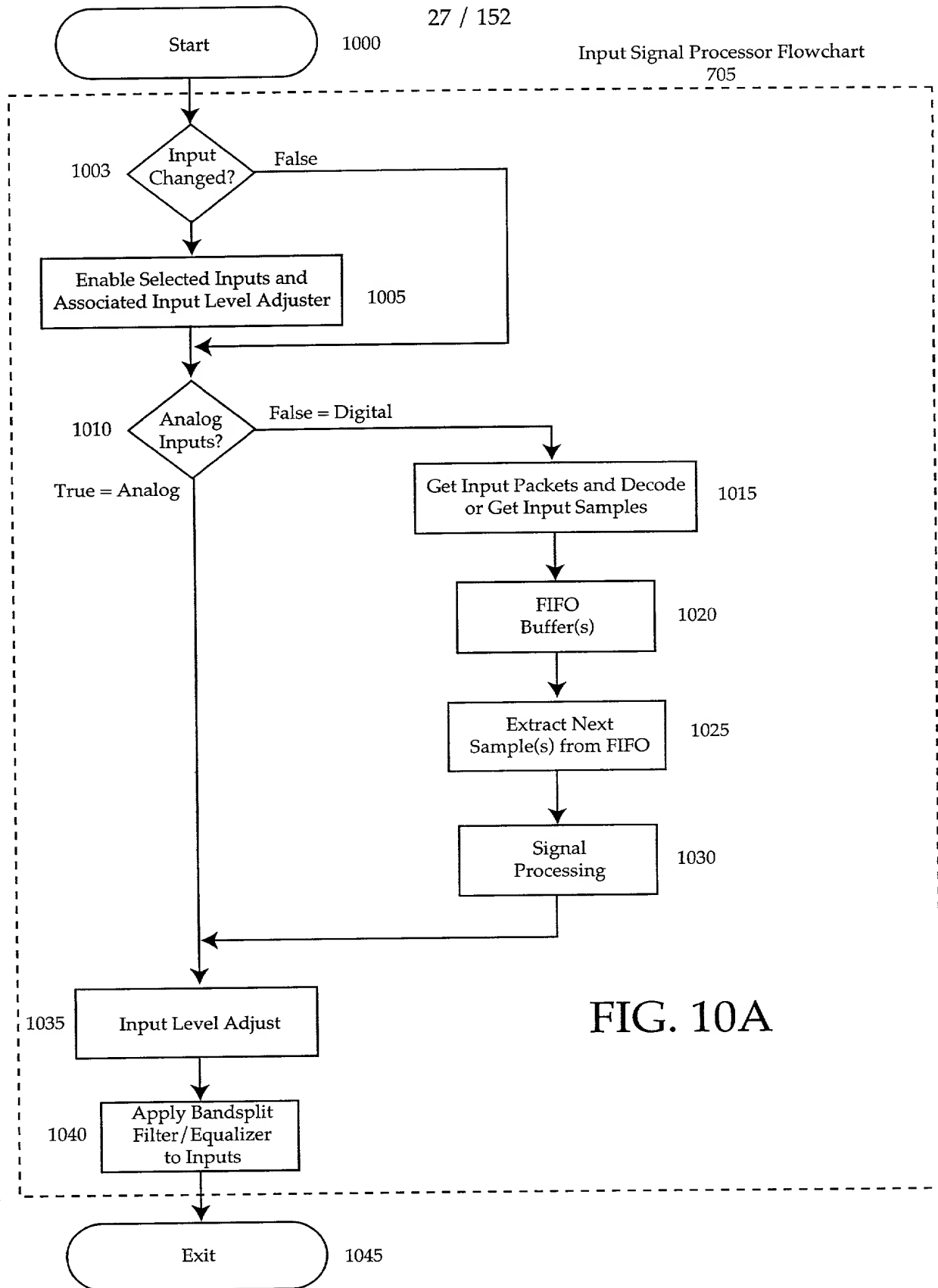


FIG. 10A

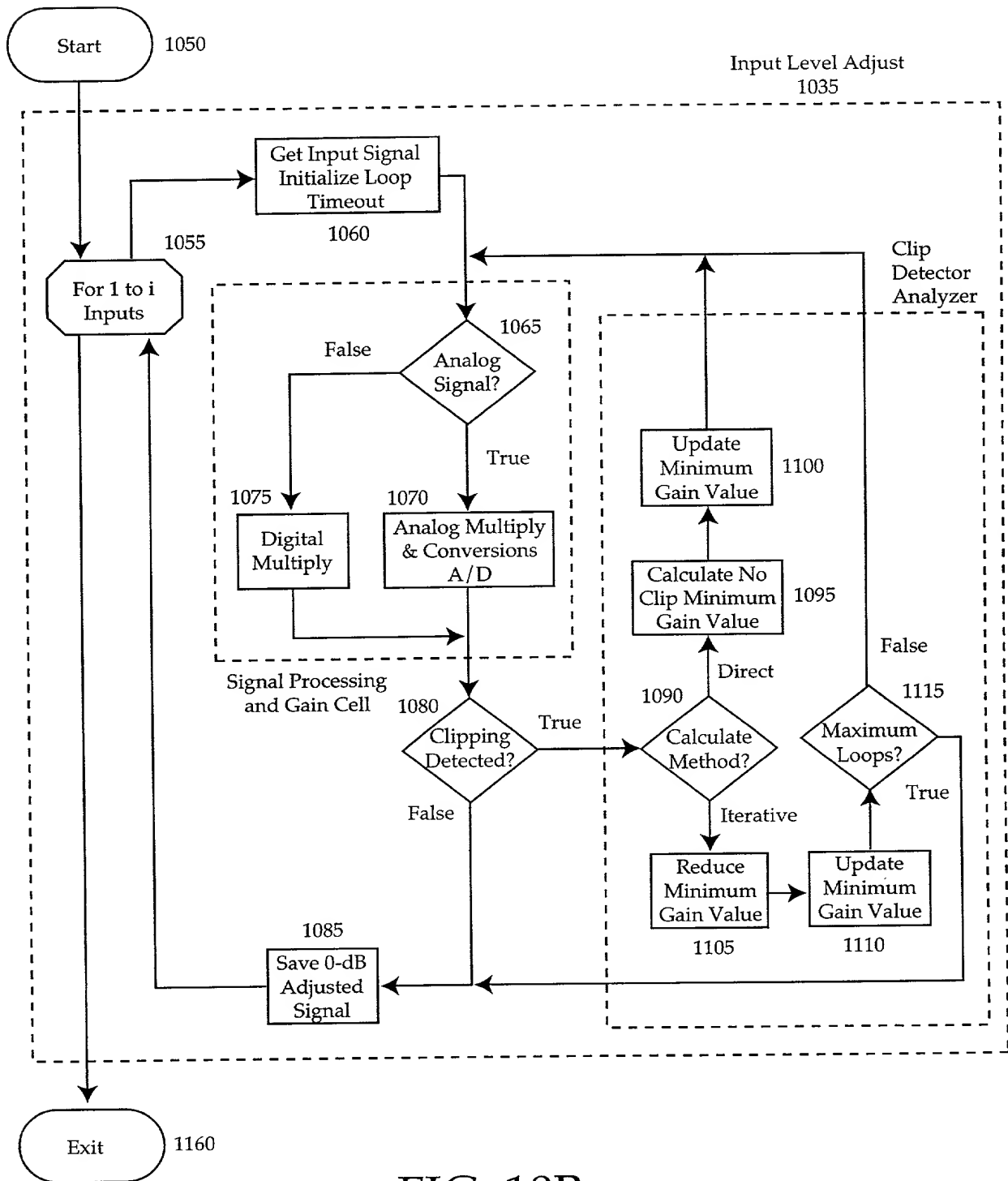


FIG. 10B

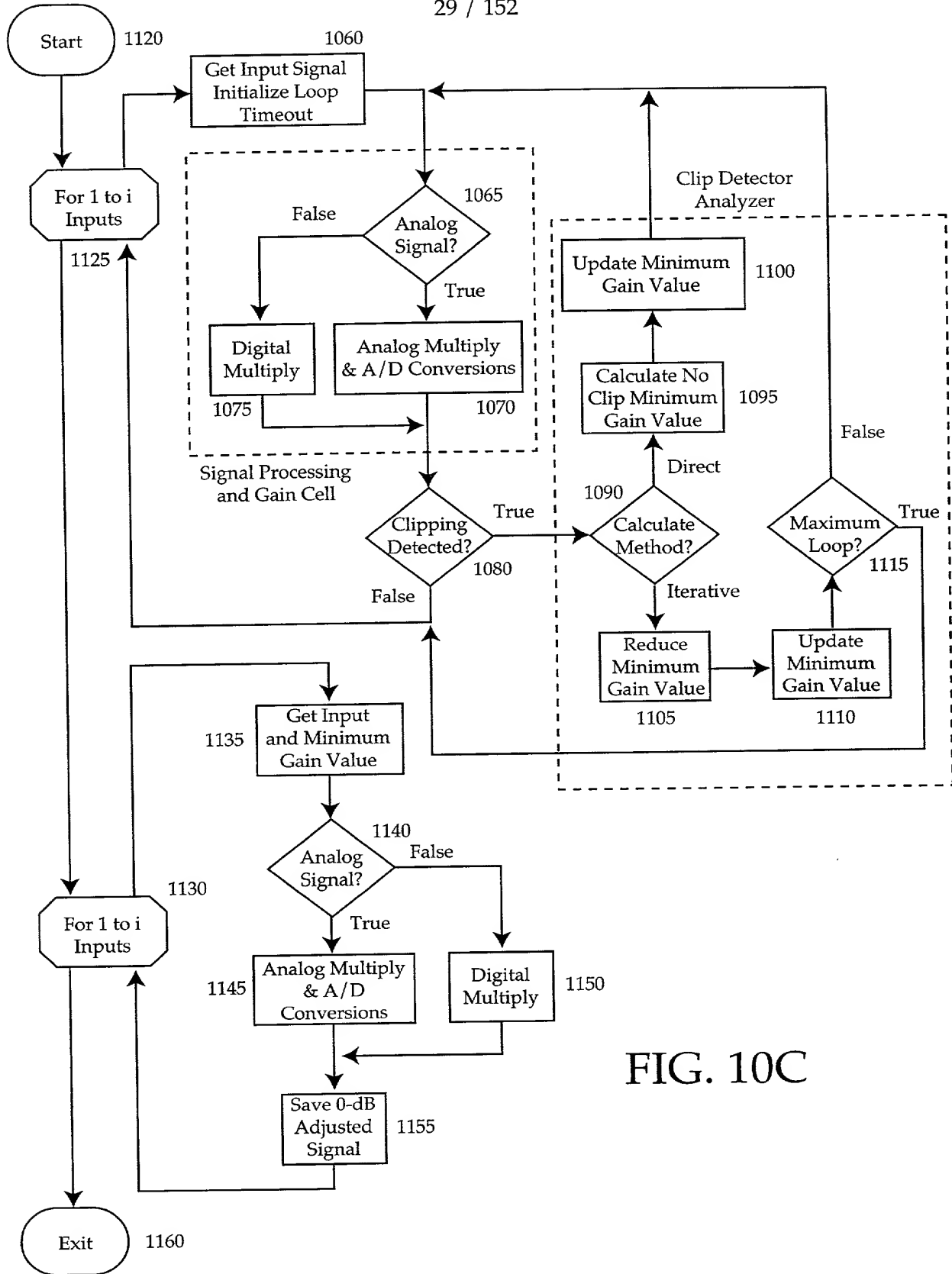


FIG. 10C

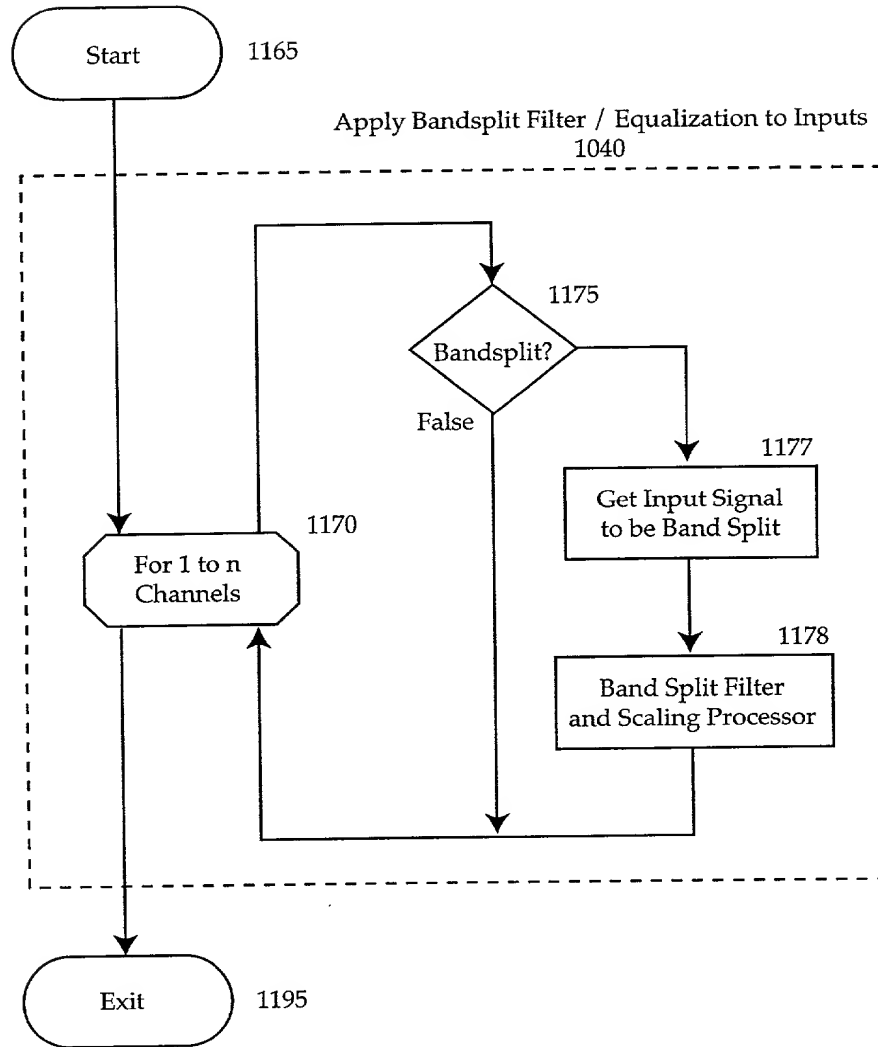


FIG. 10D

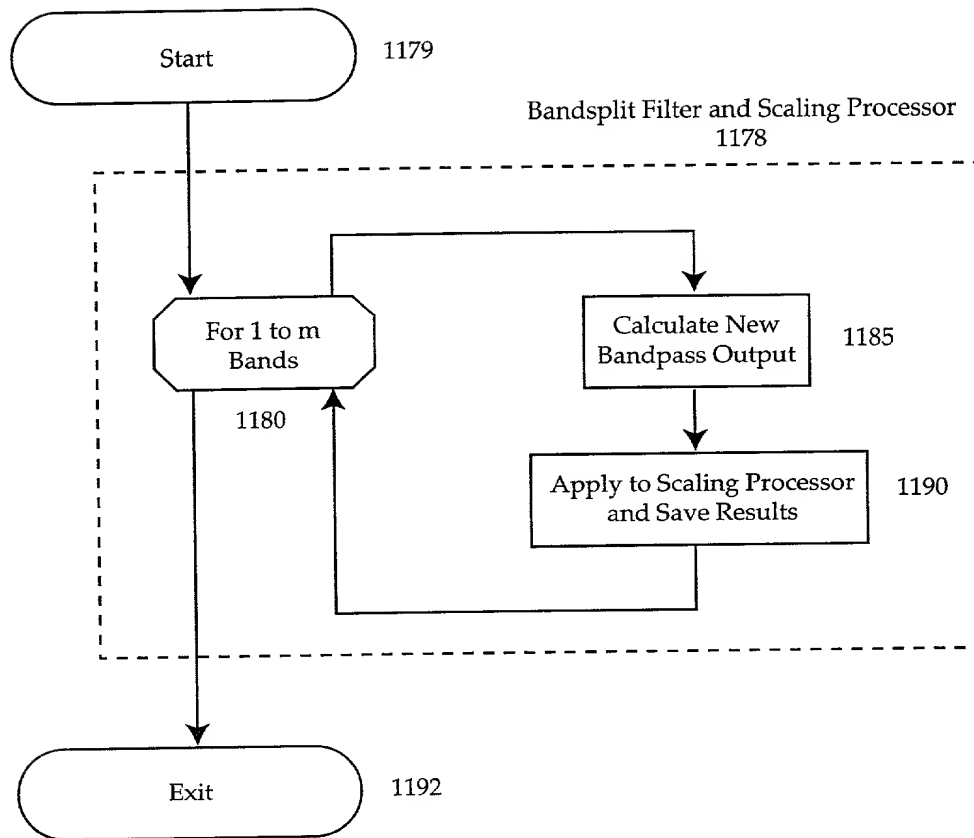


FIG. 10E

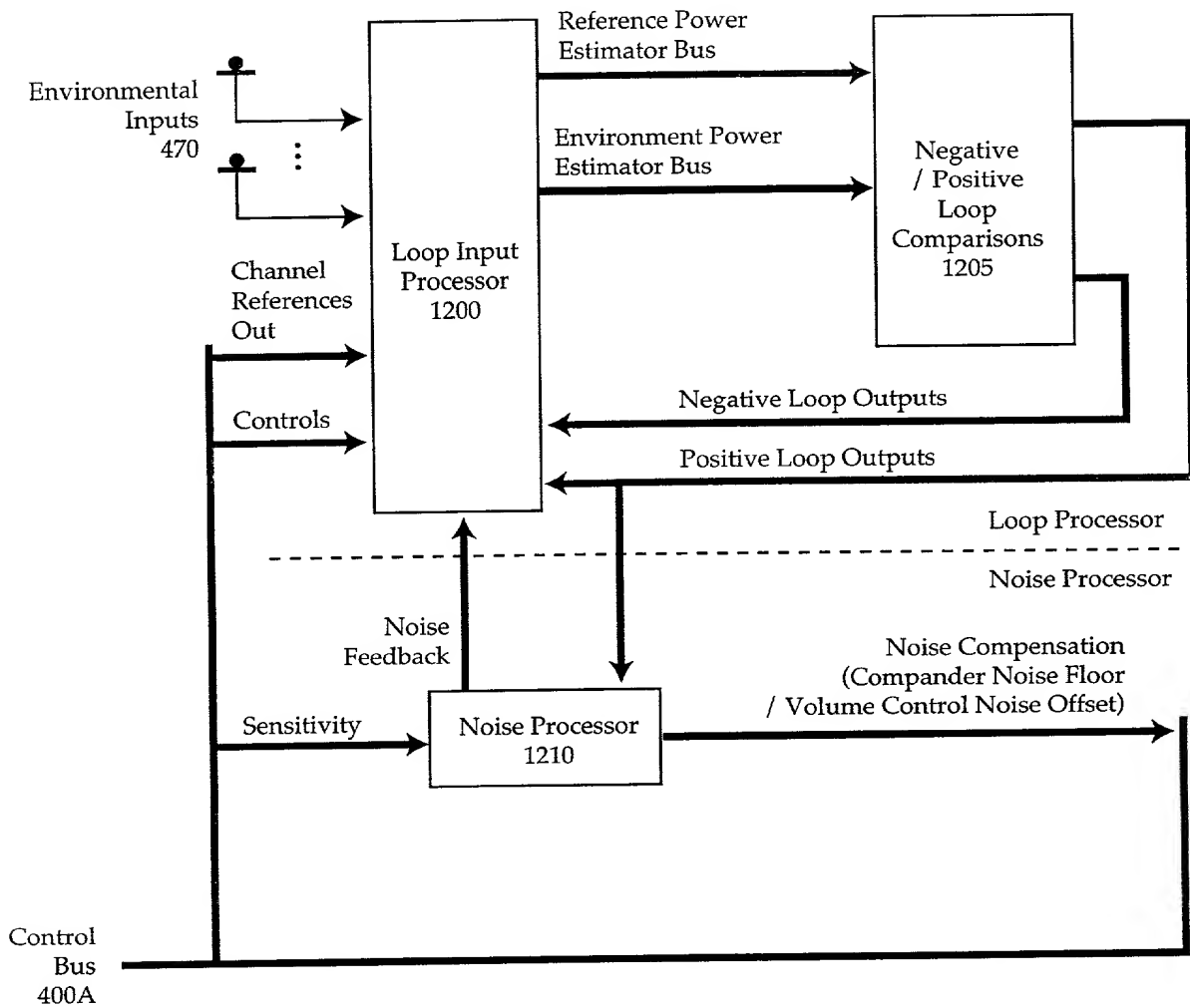


FIG. 11

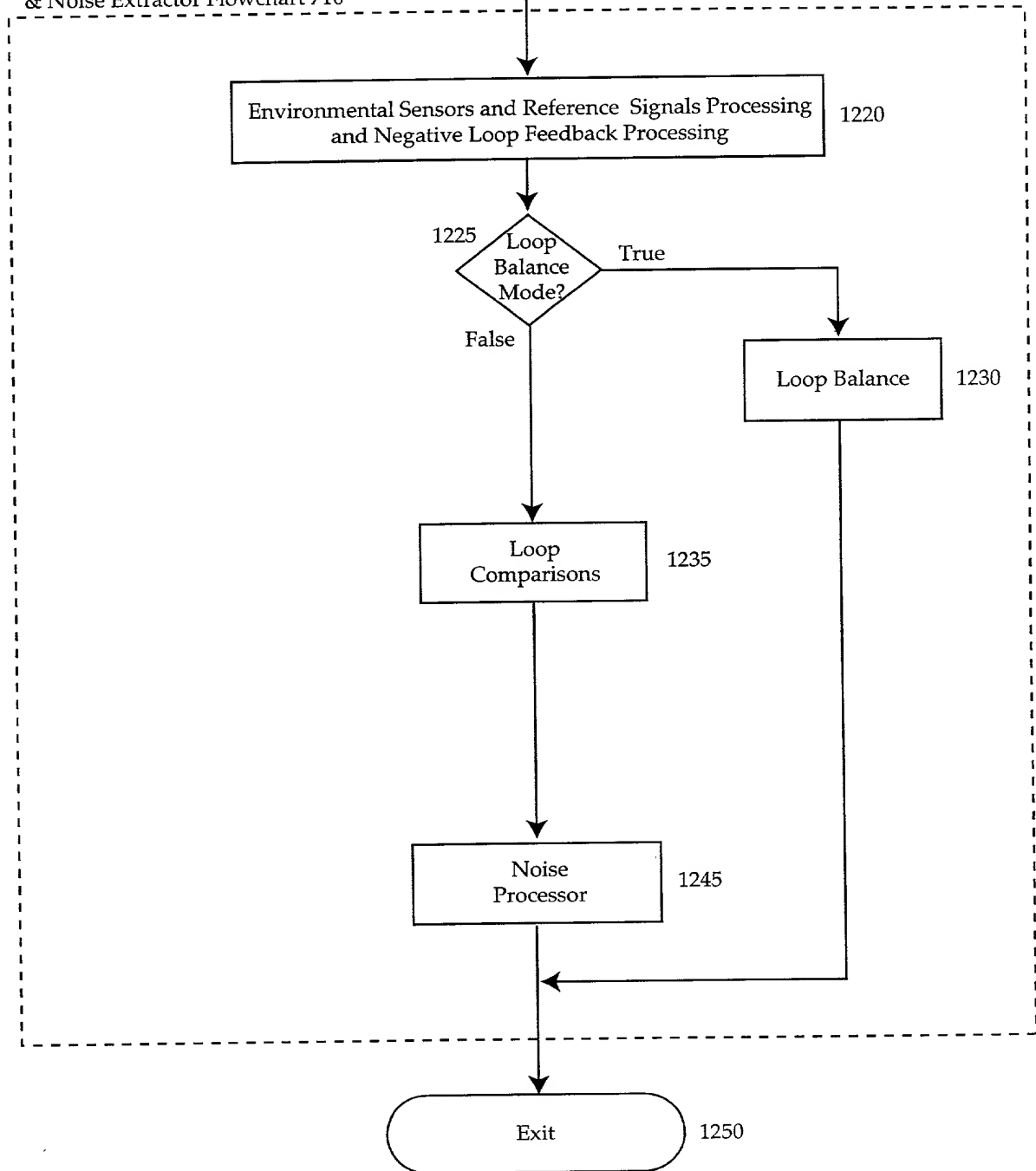
Environmental Sensor Adjustments
& Noise Extractor Flowchart 710

FIG. 12

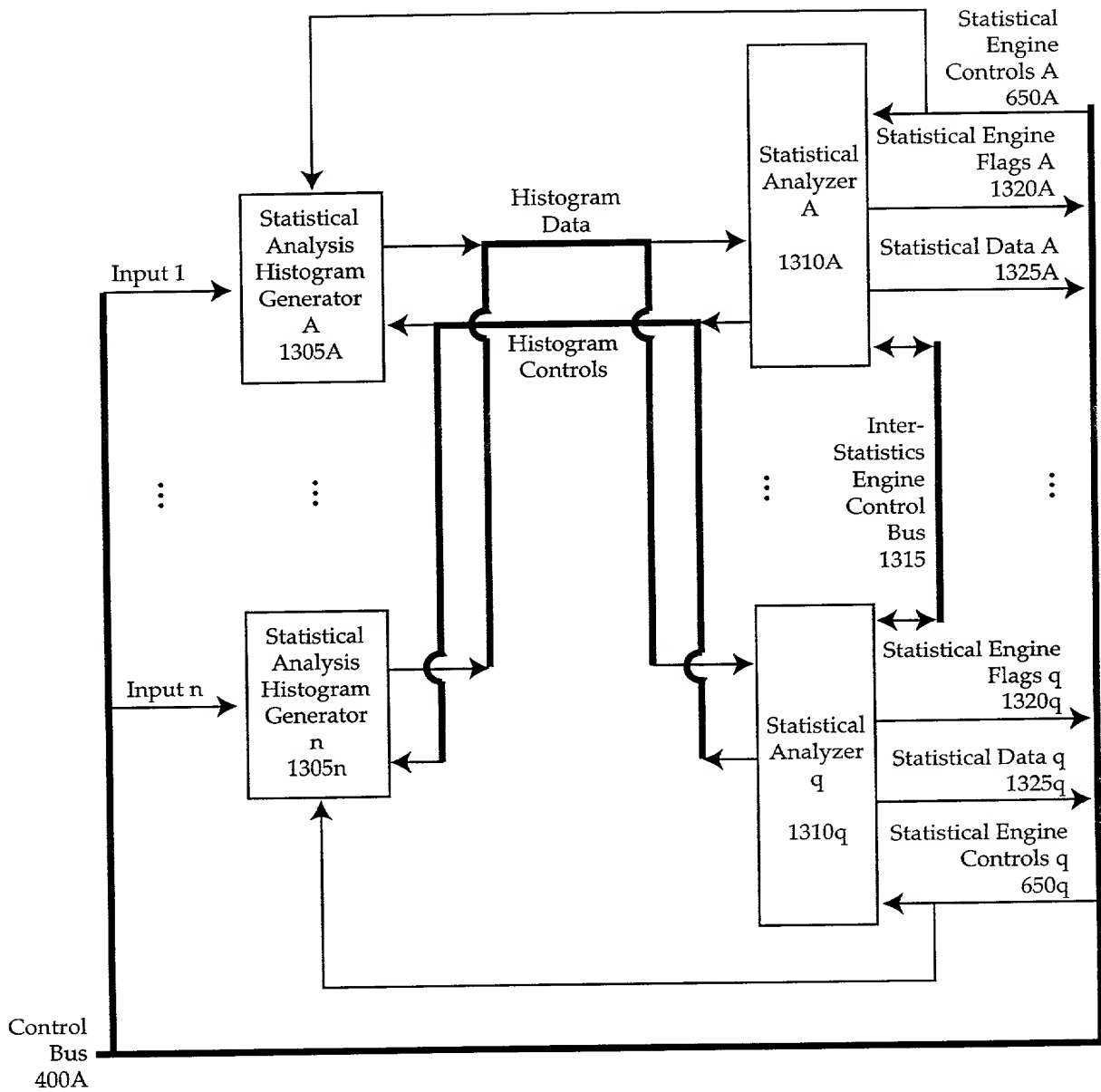


FIG. 13

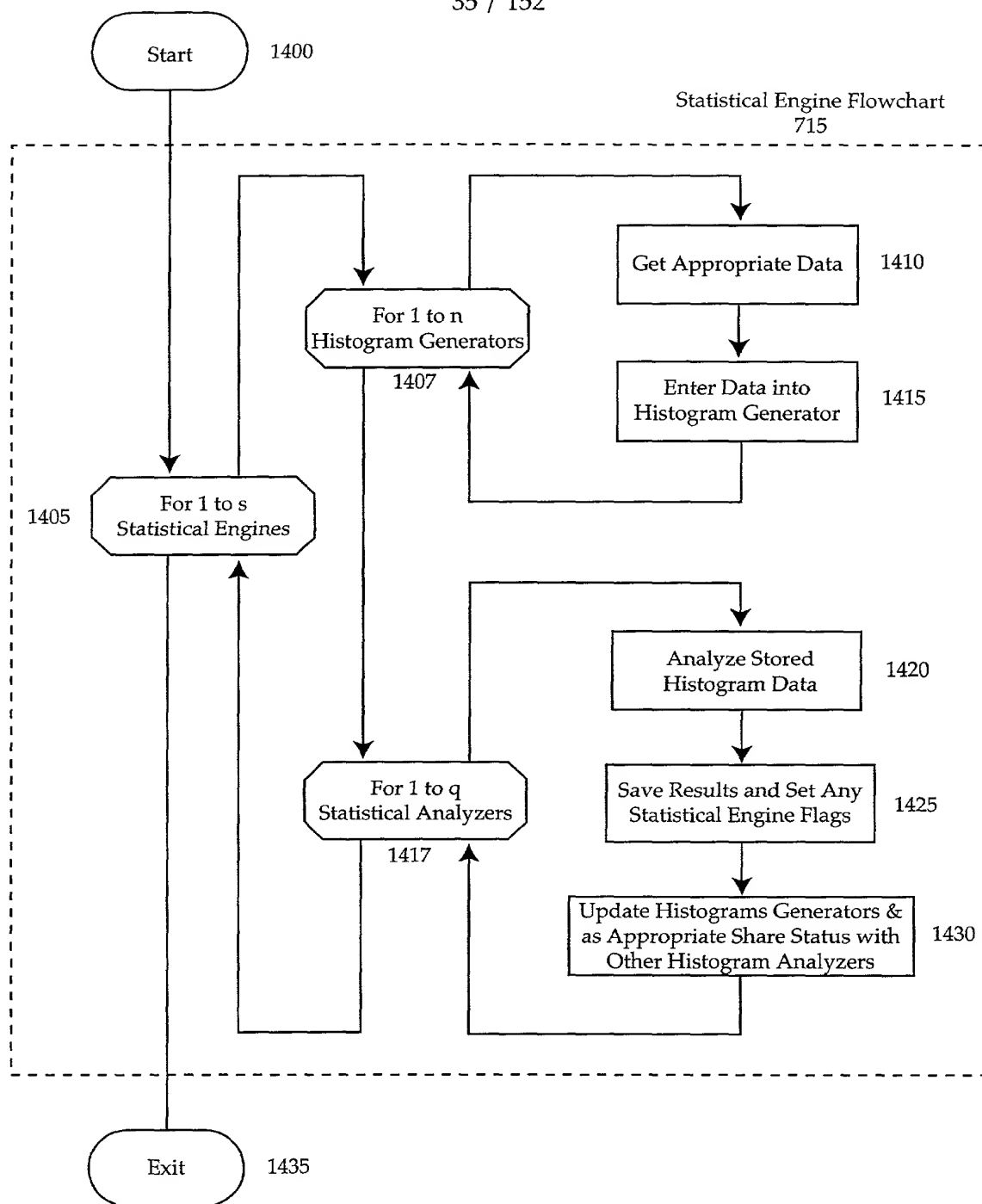


FIG. 14

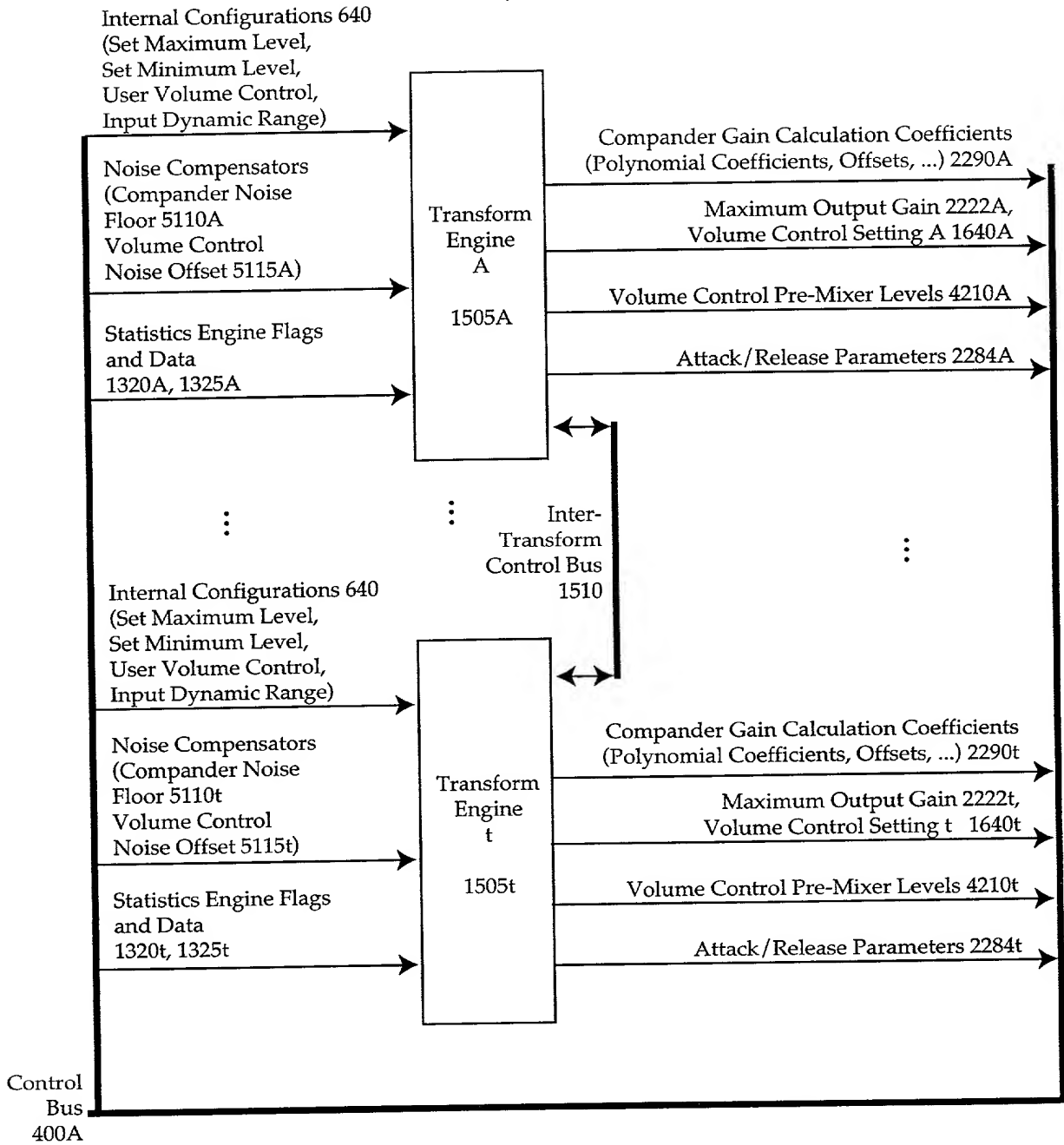


FIG. 15

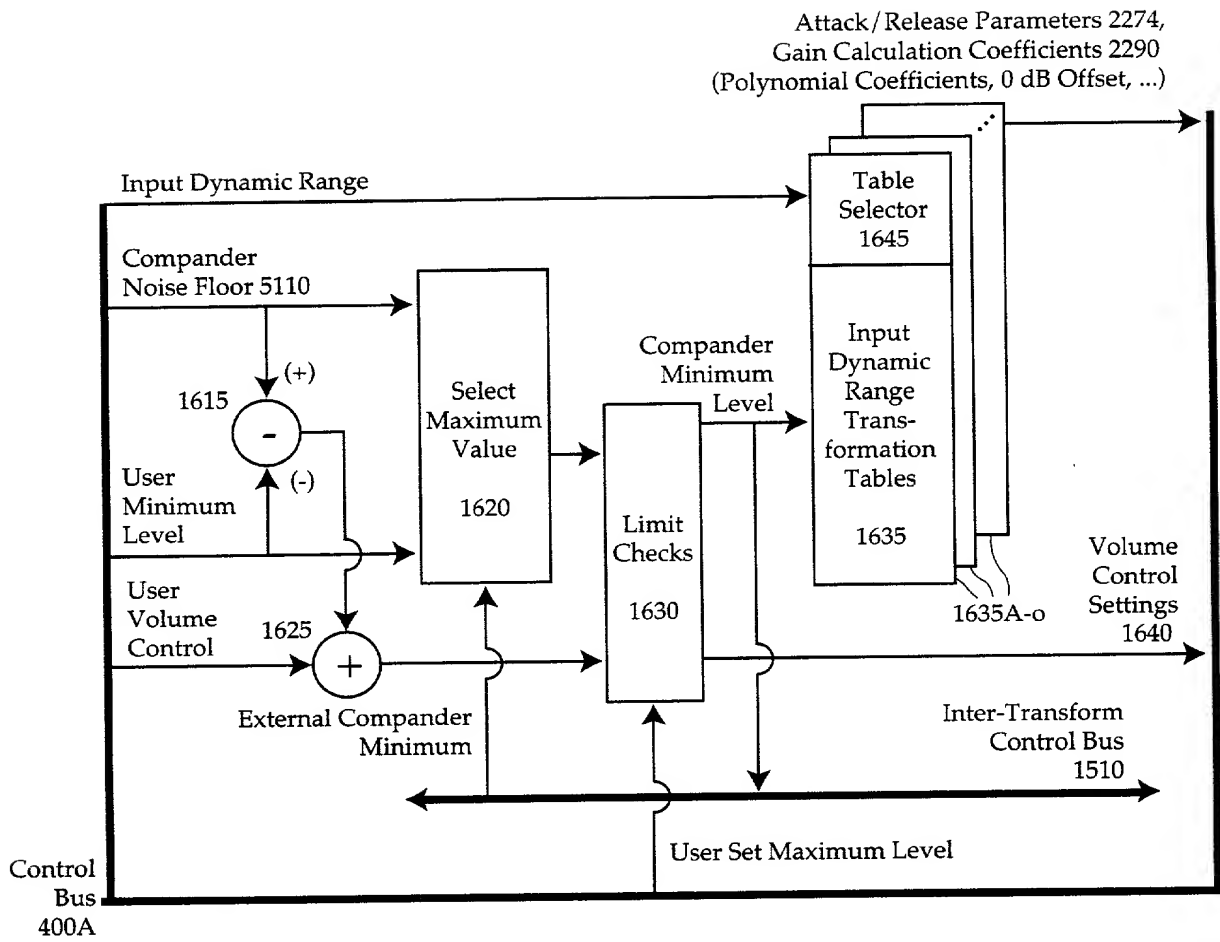


FIG. 16

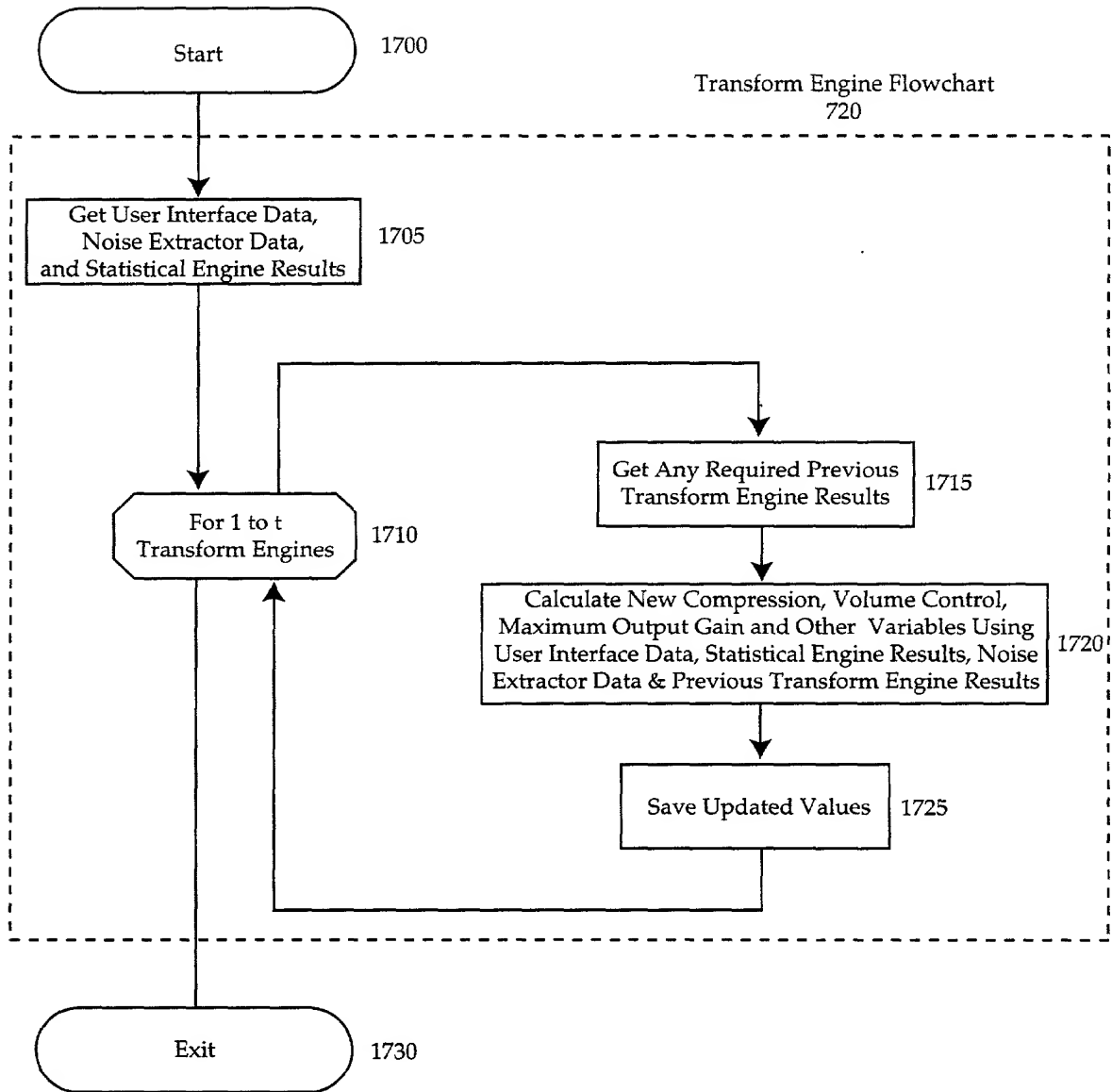


FIG. 17

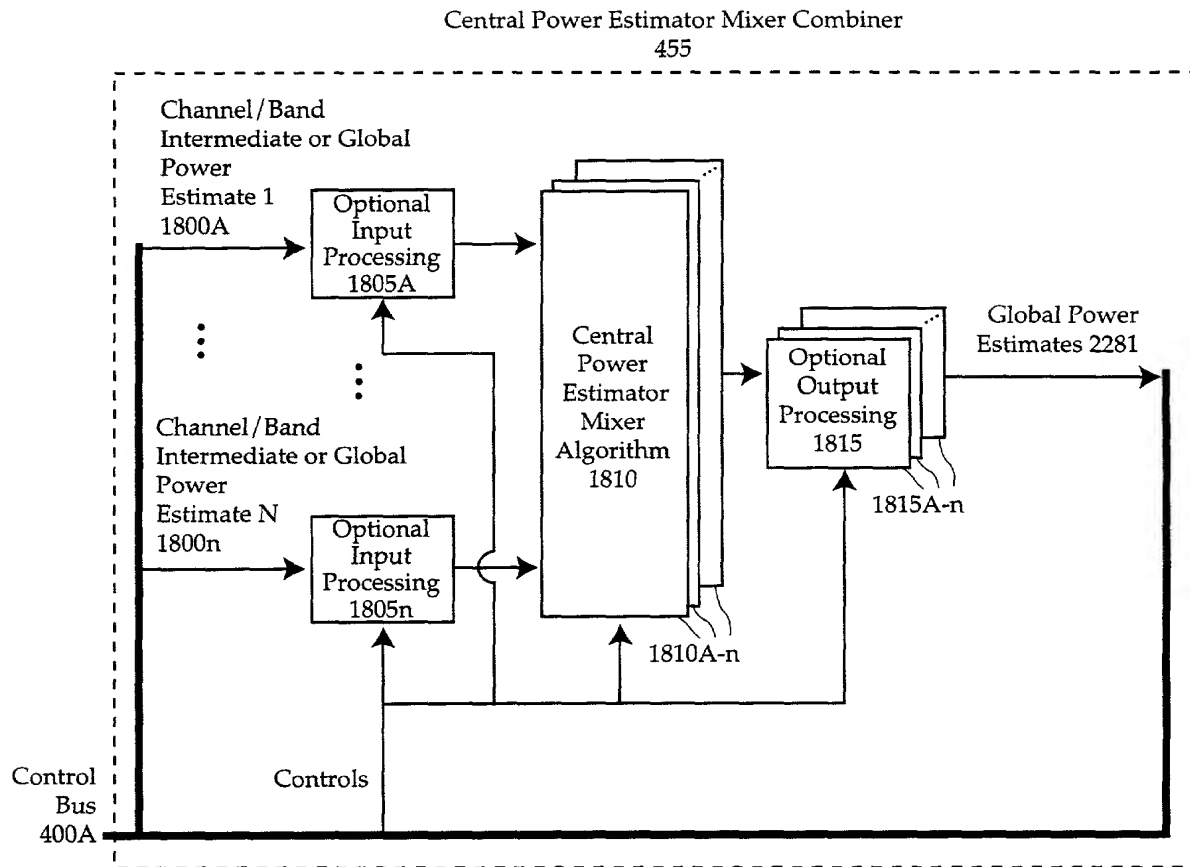


FIG. 18

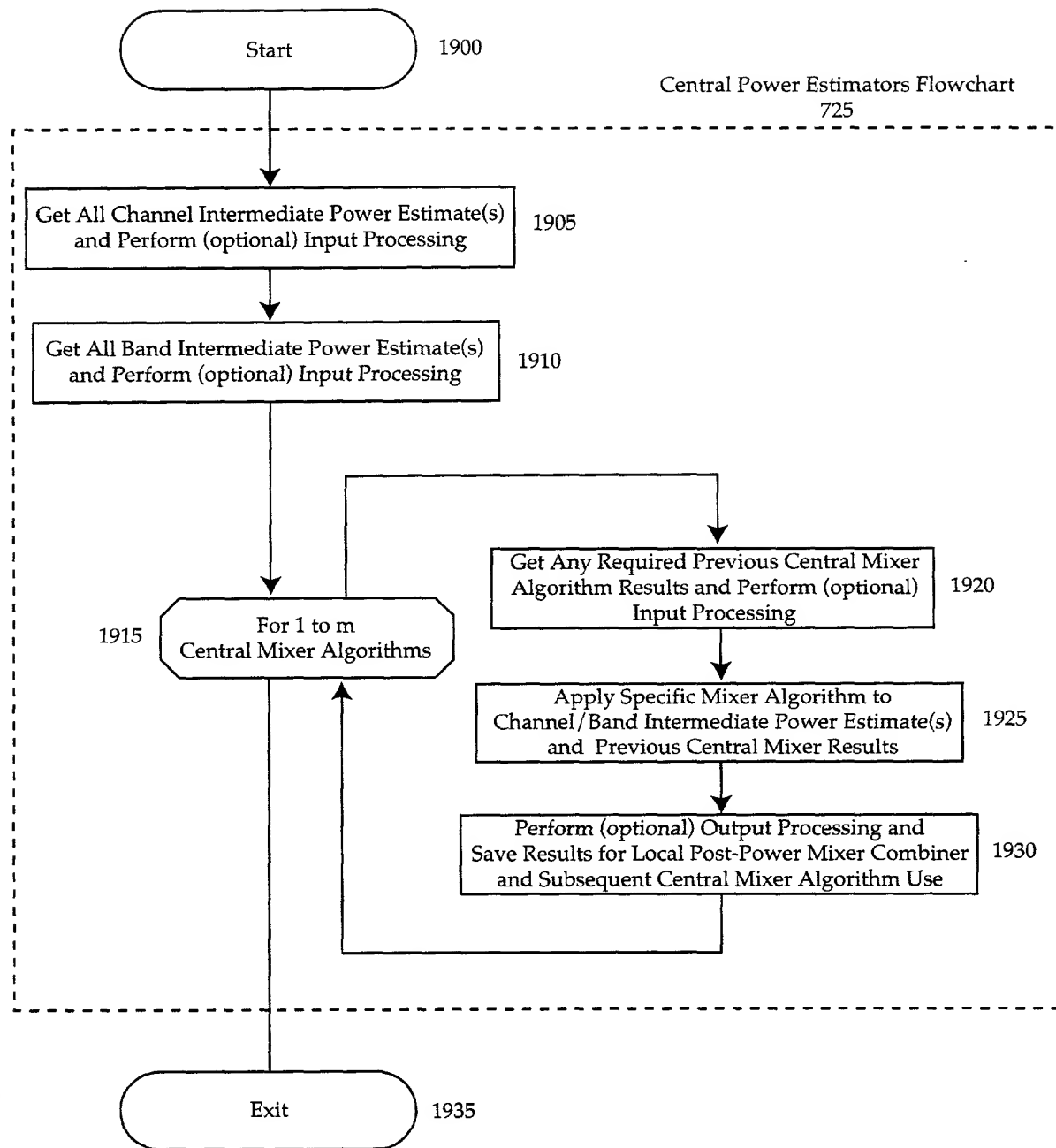
Central Power Estimators Flowchart
725

FIG. 19

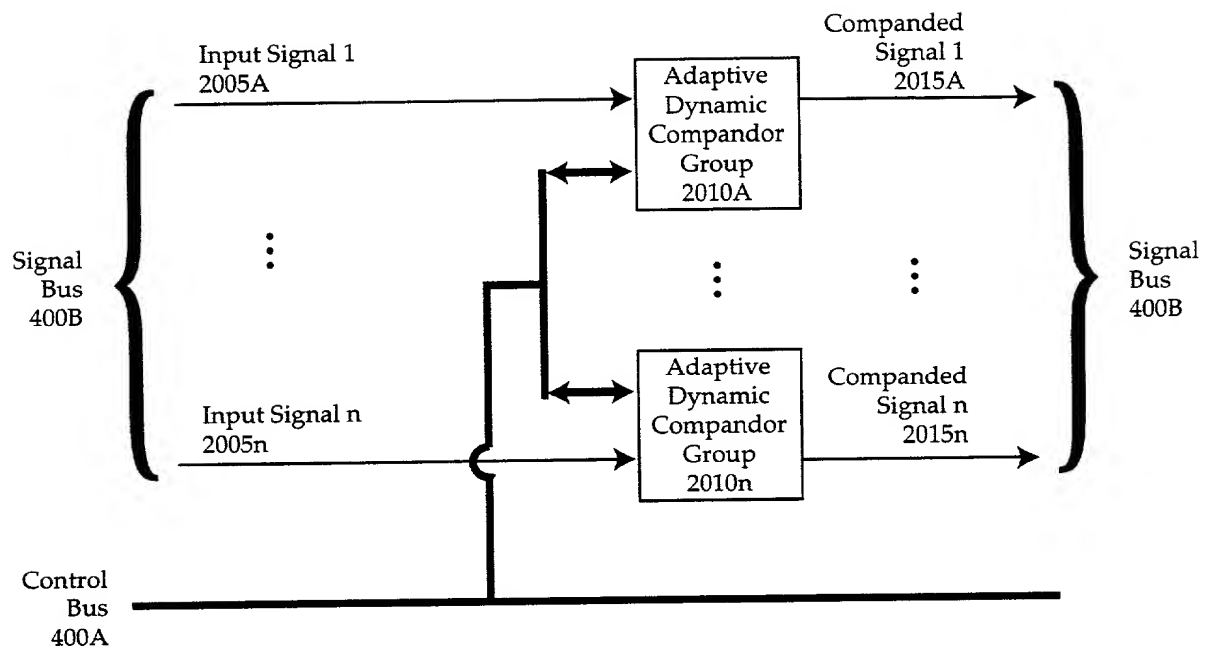


FIG. 20A

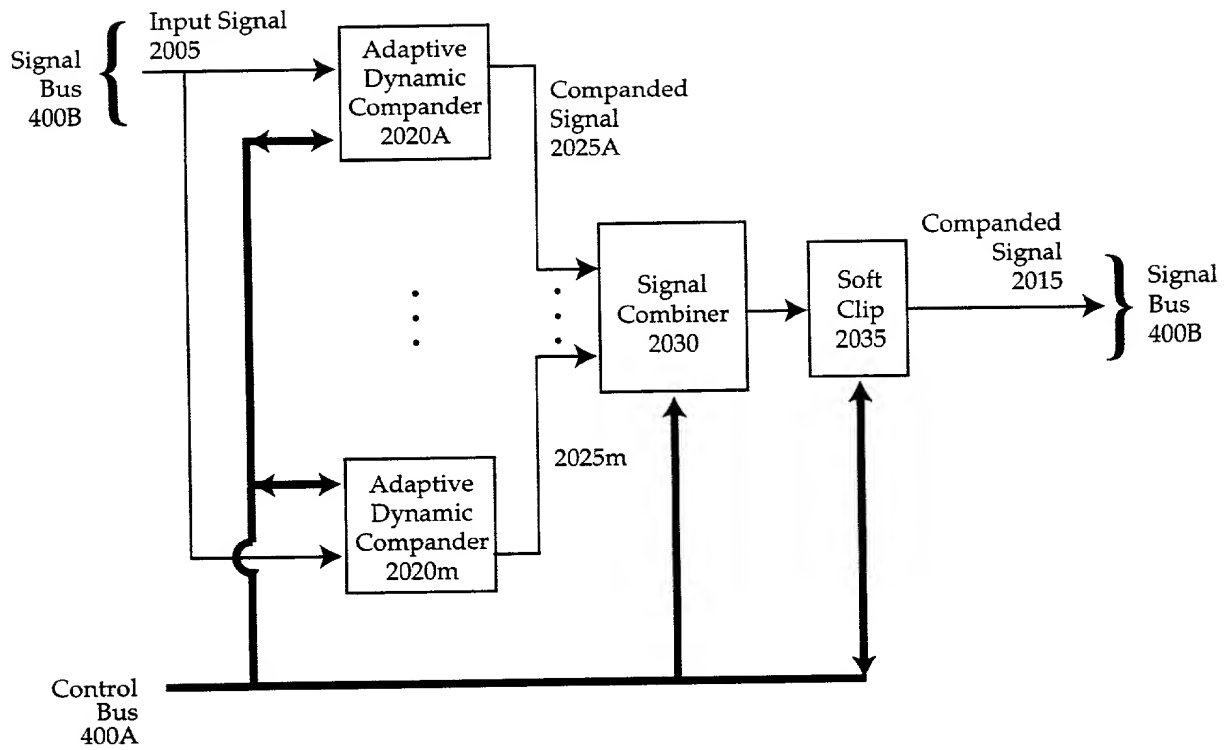


FIG. 20B

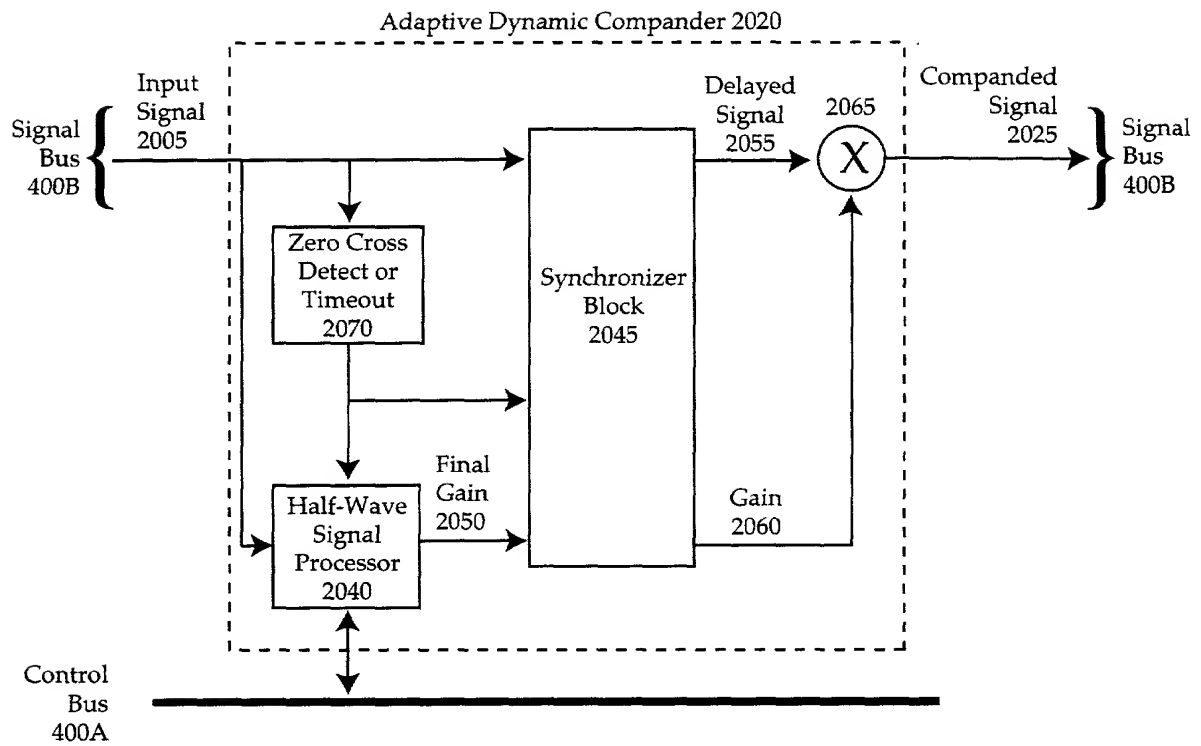


FIG. 20C

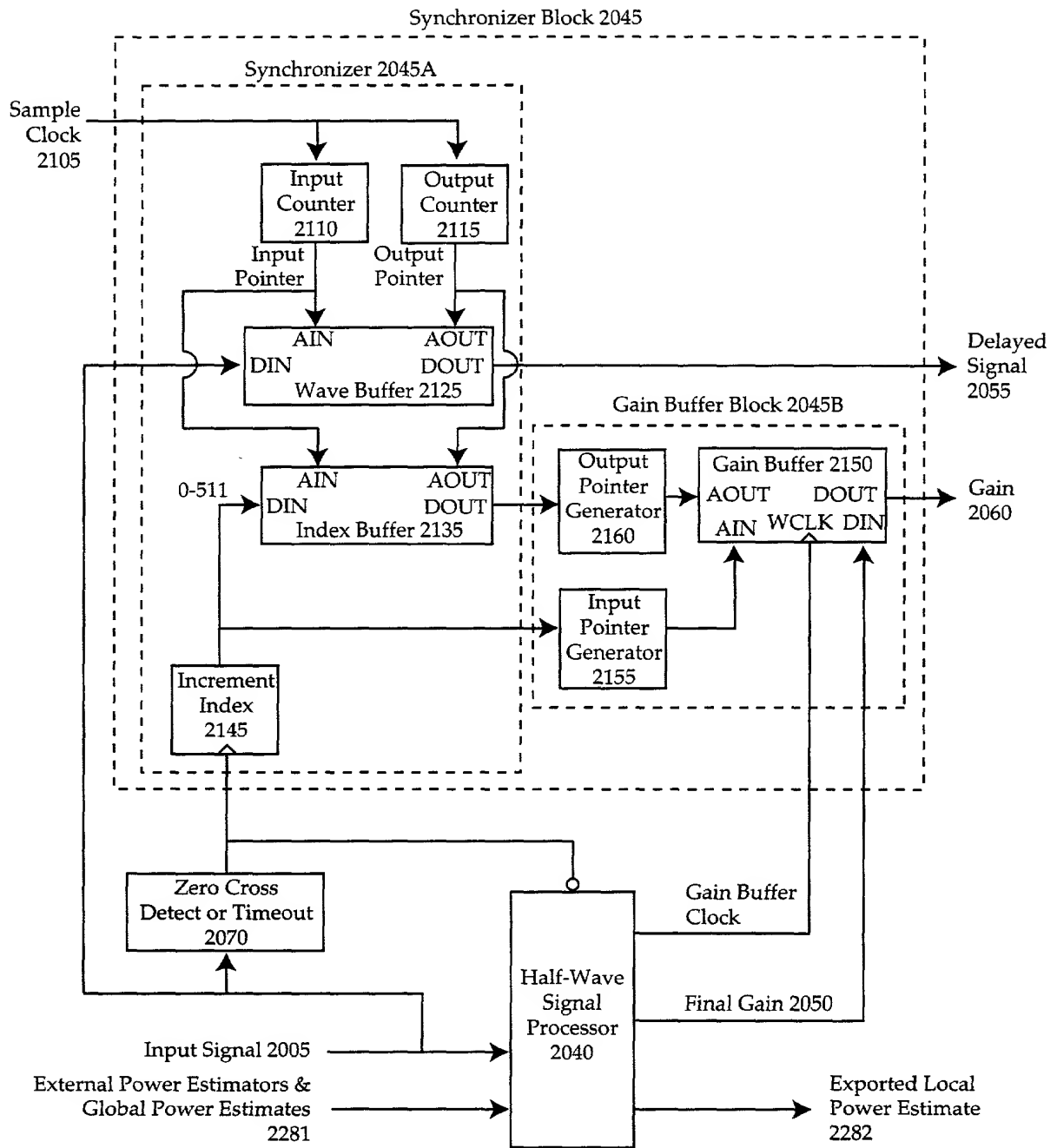


FIG. 21A

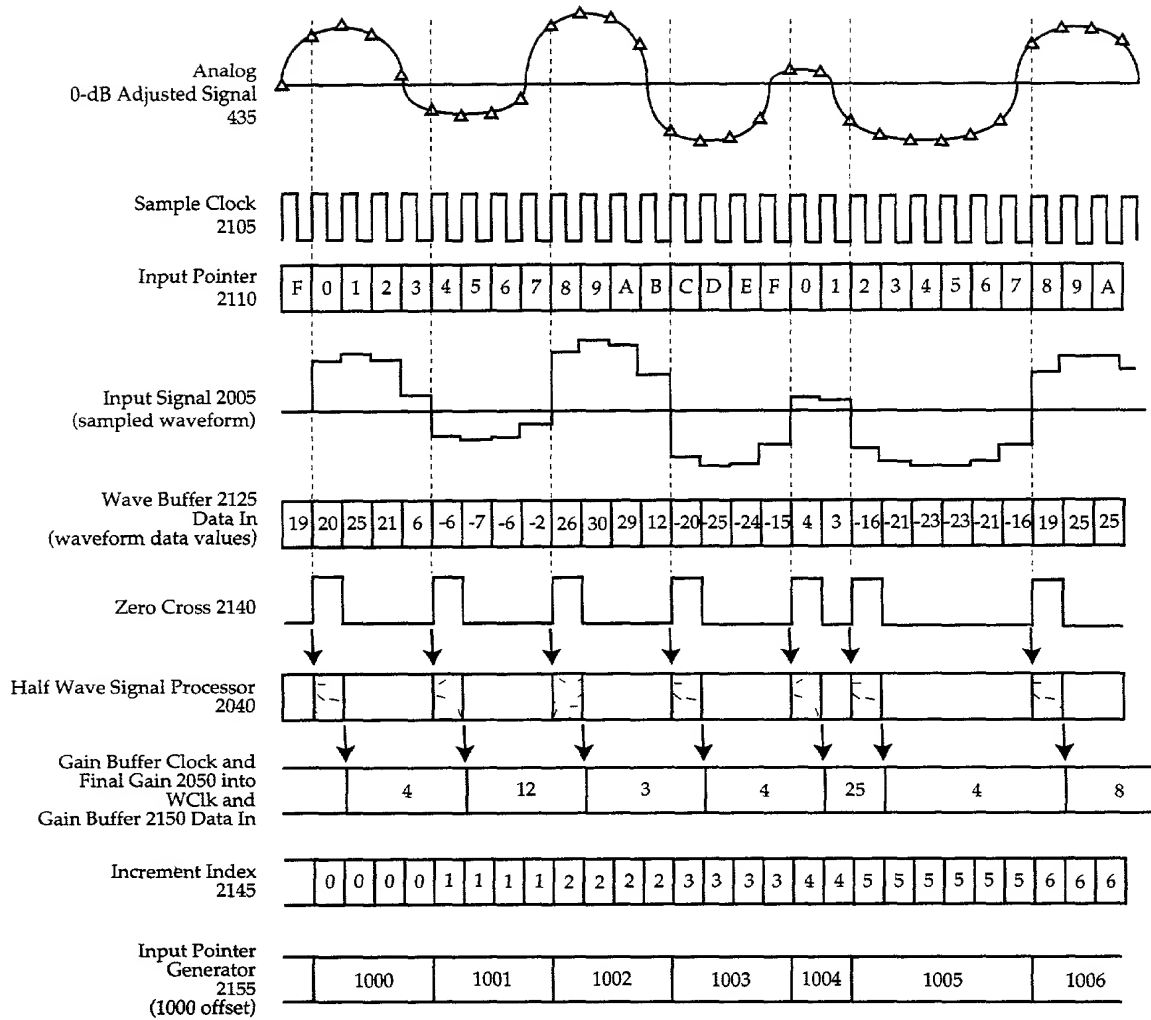


FIG. 21B

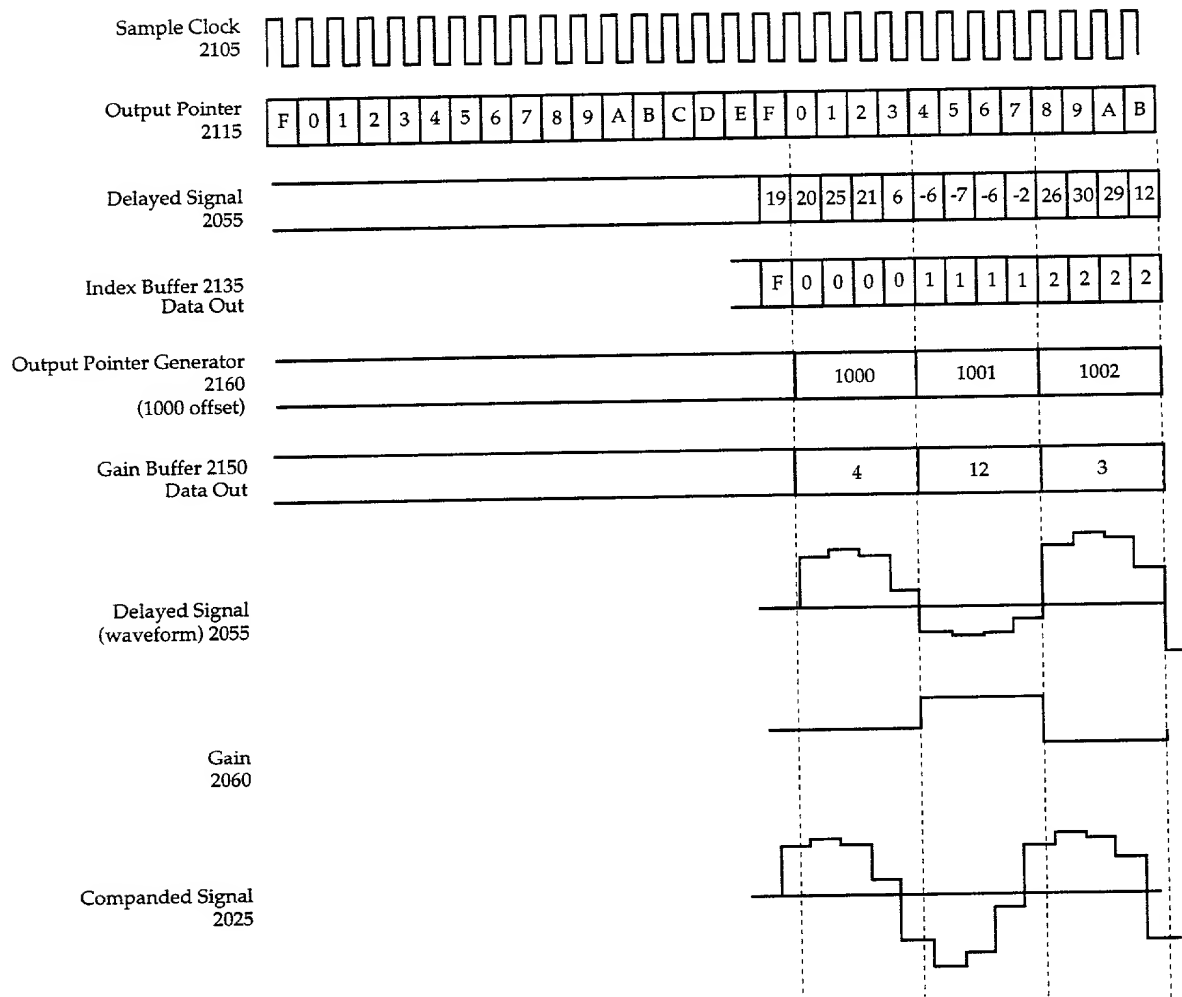


FIG. 21C

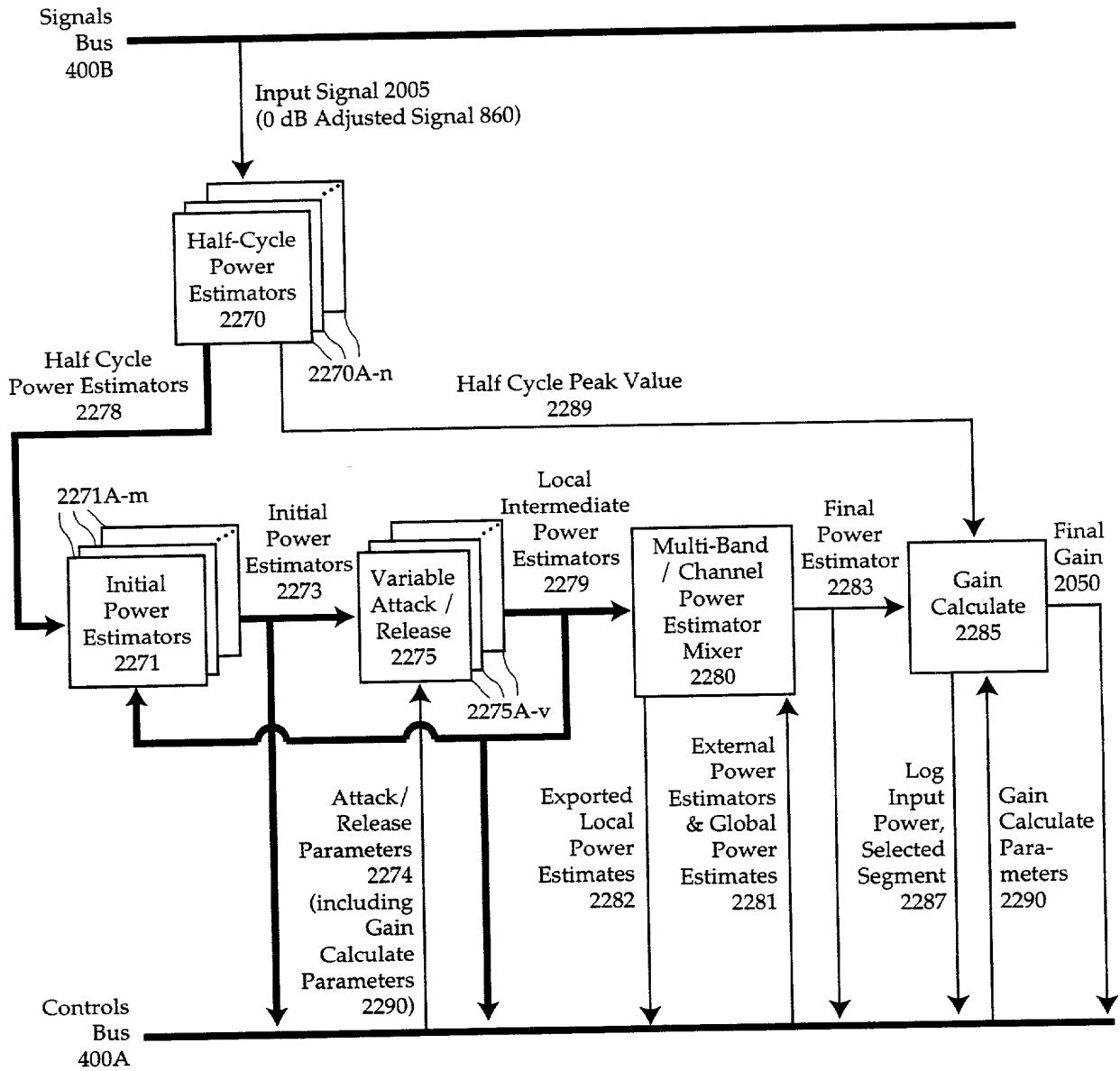


FIG. 22

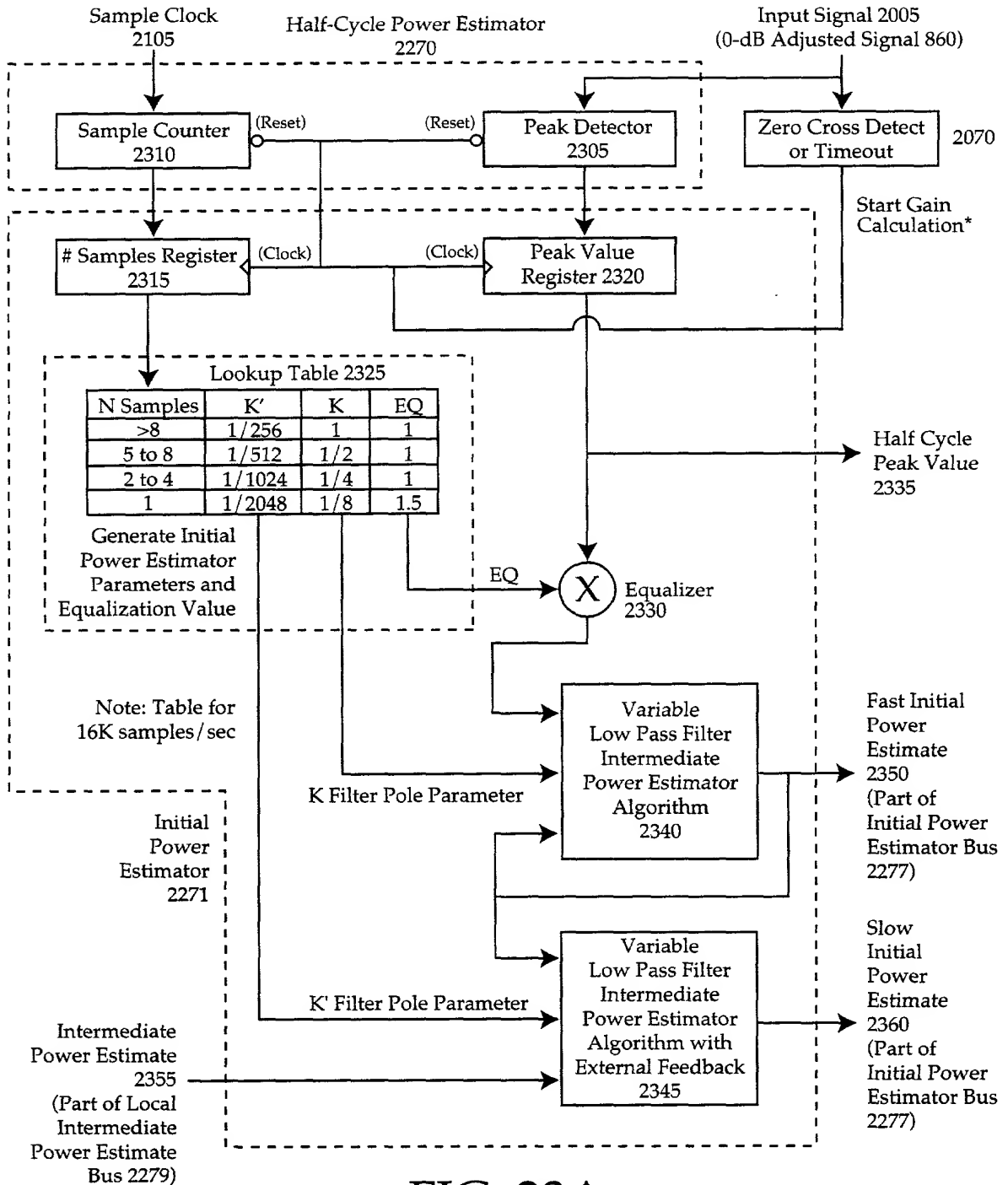


FIG. 23A

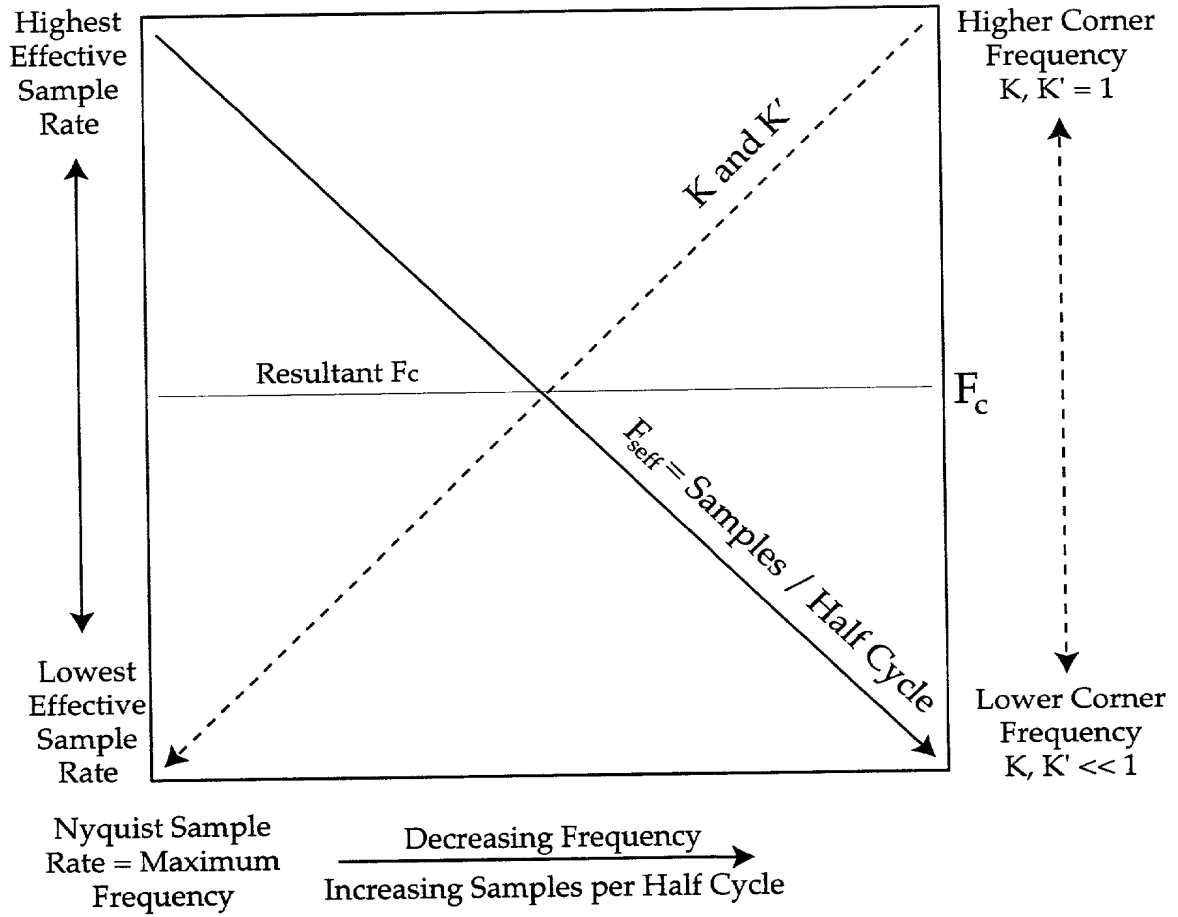
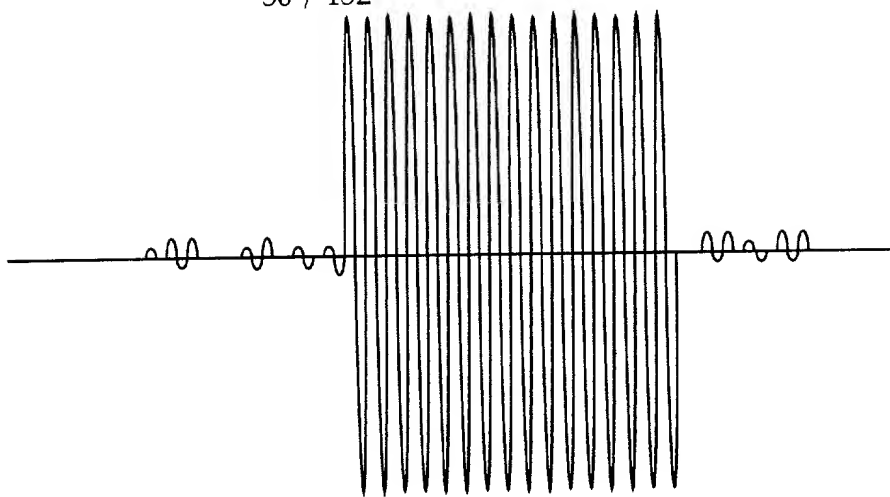


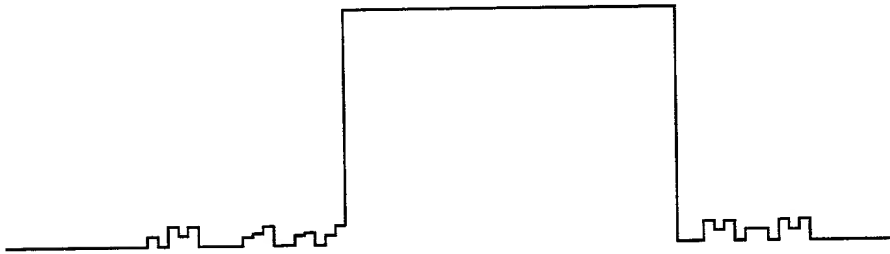
FIG. 23B

Input Signal
2005
(0-dB Adjusted
Signal 860)

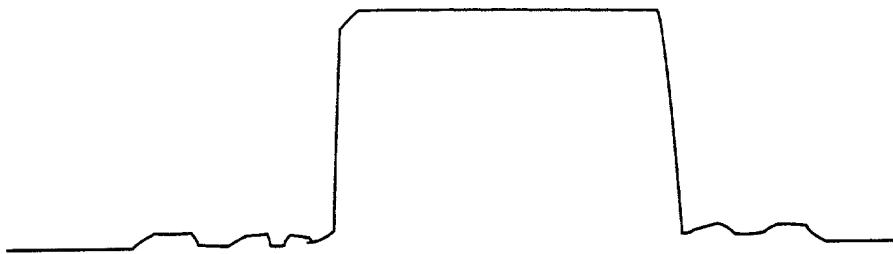
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Half Cycle
Peak Value
2289



Fast Initial
Power Estimate
2350



Intermediate
Power
Estimate
2355

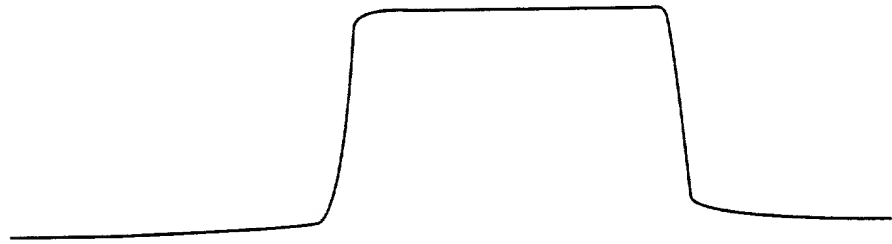


FIG. 23C

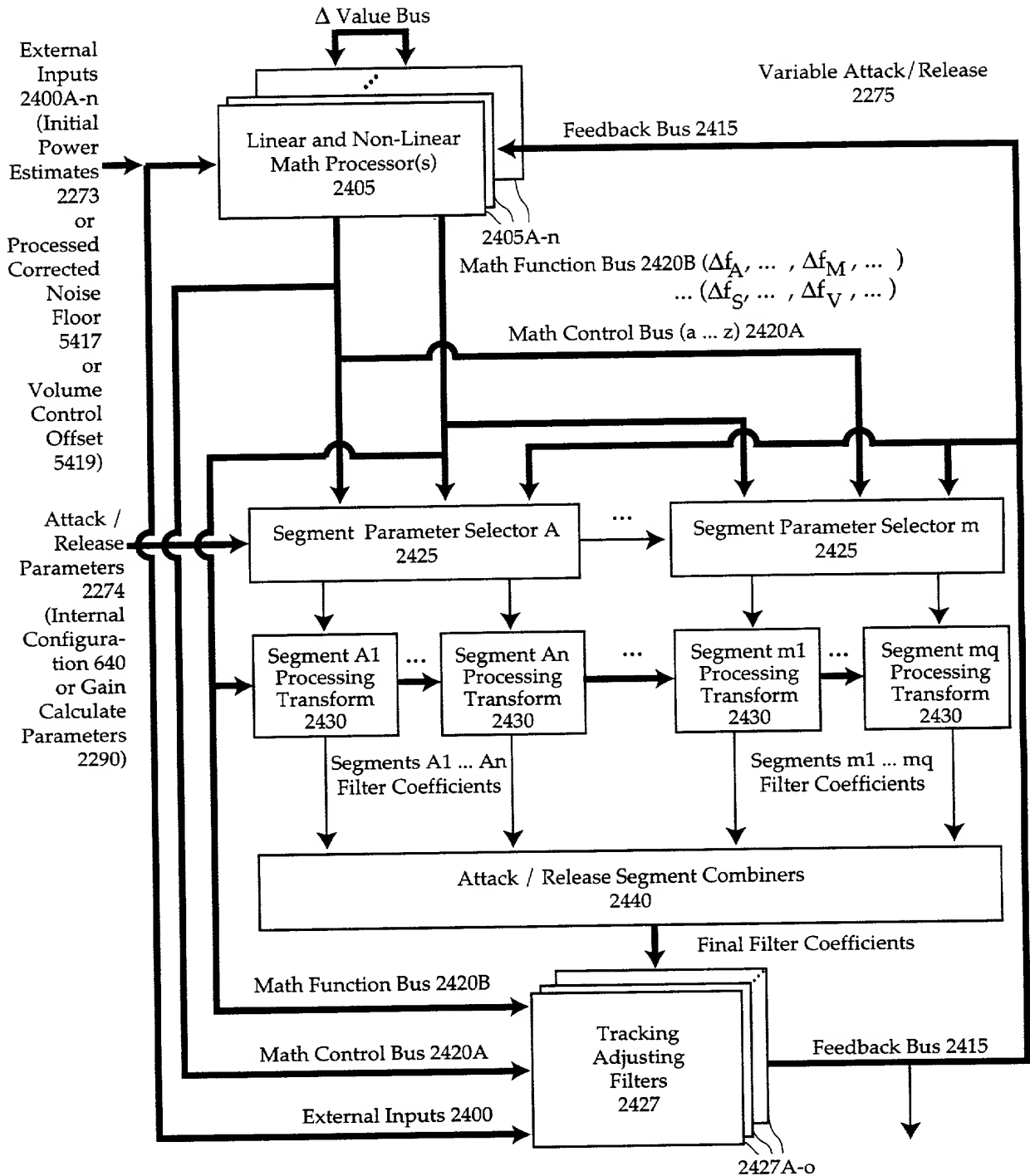


FIG. 24A

Local Intermediate Power Estimates 2279
or Long Duration Noise Floor 5425
or Long Duration Noise Offset 5427

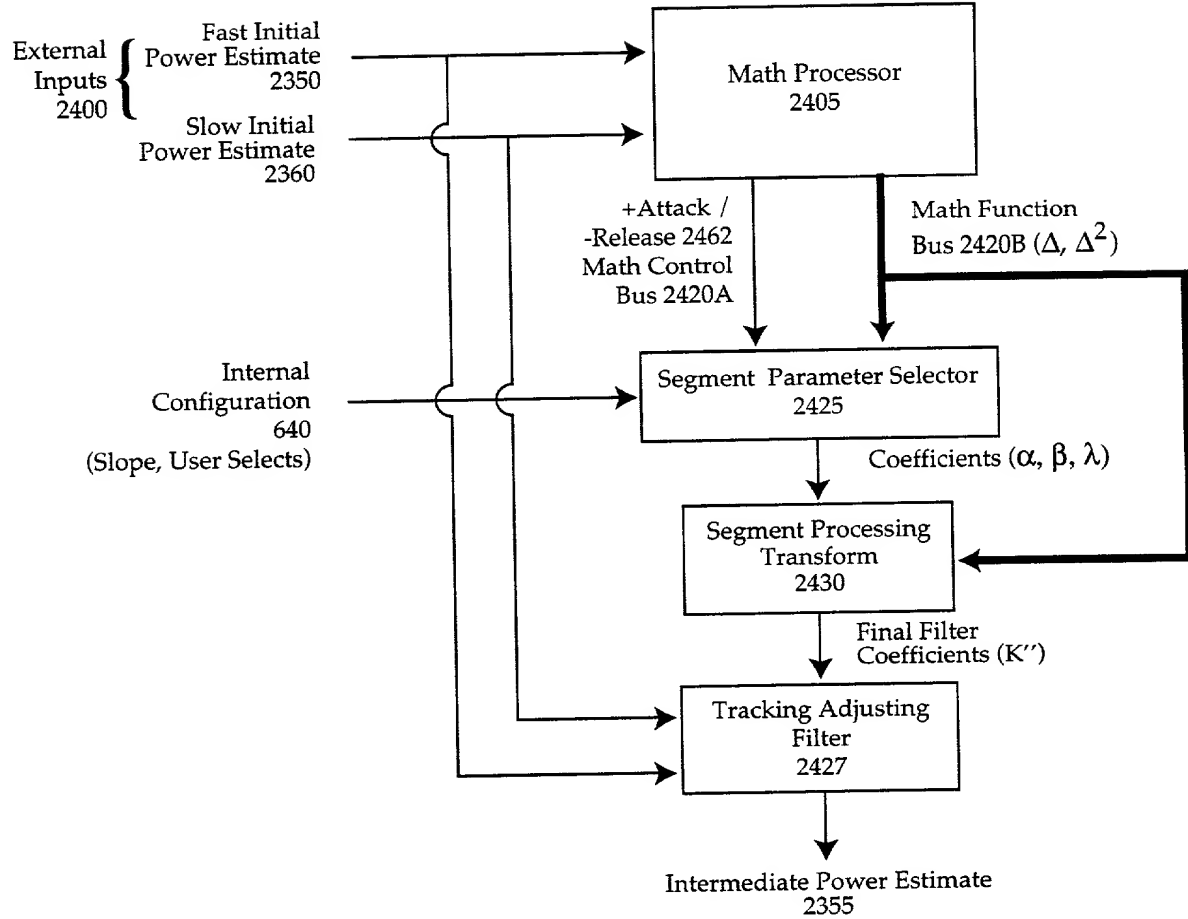
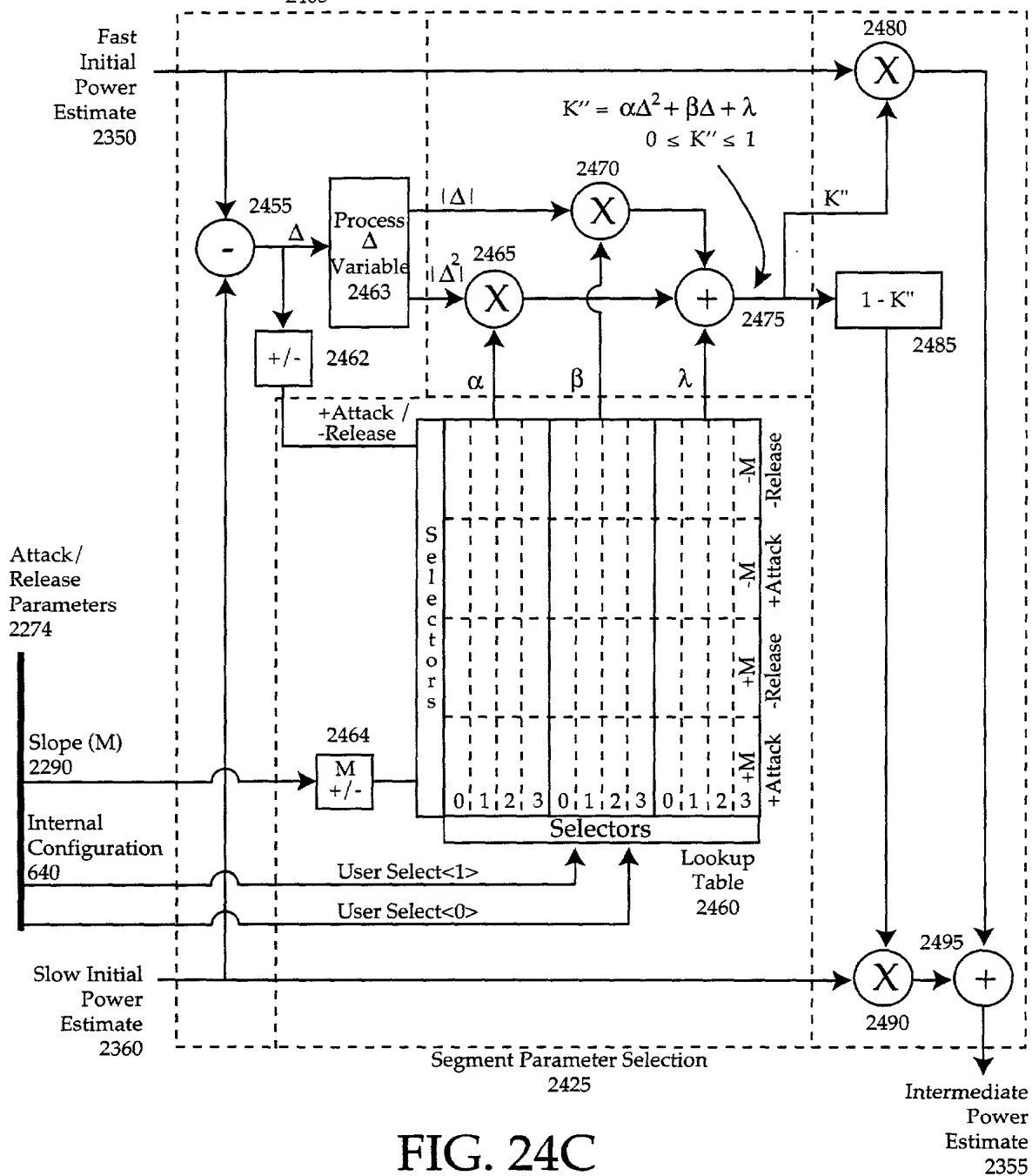


FIG. 24B

Math Processors
2405Segment Processing Transform
2430Tracking Adjuster
Filter 2427

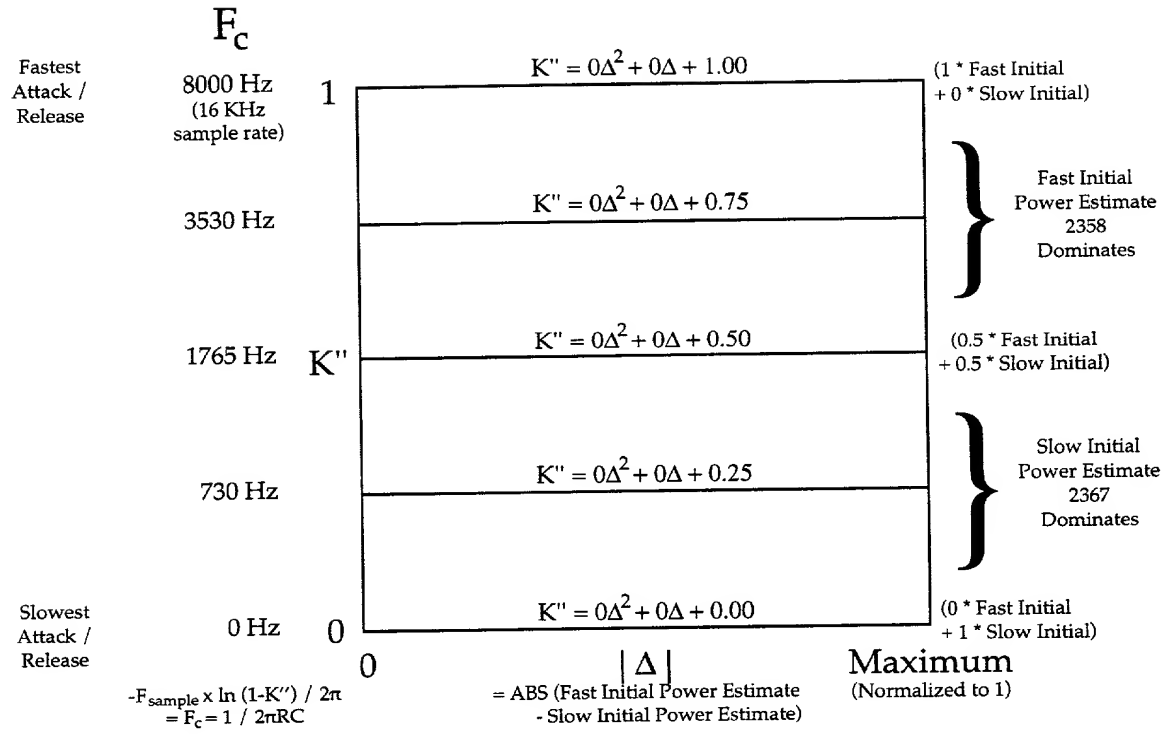


FIG. 24D

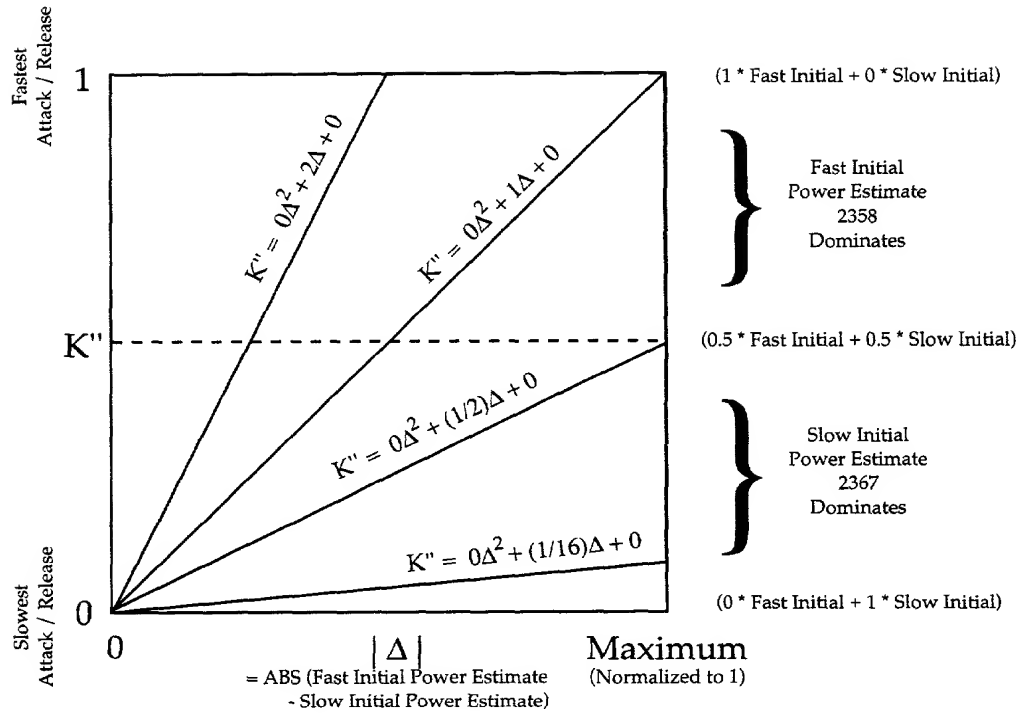


FIG. 24E

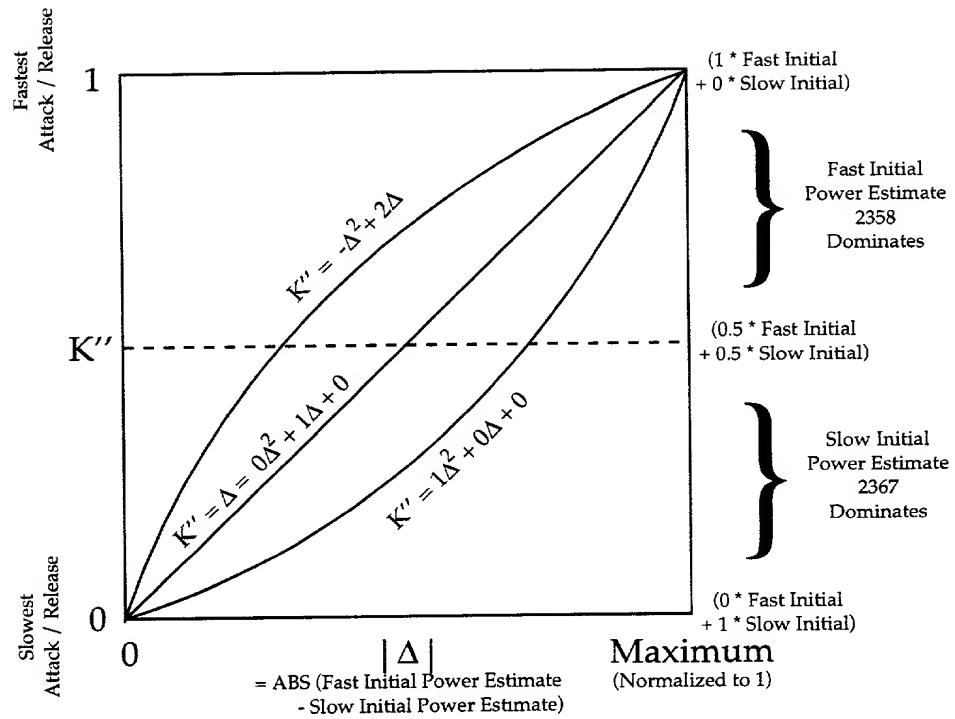


FIG. 24F

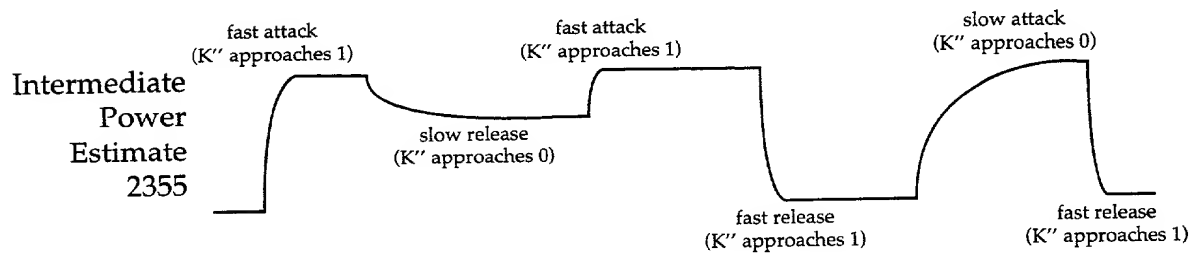
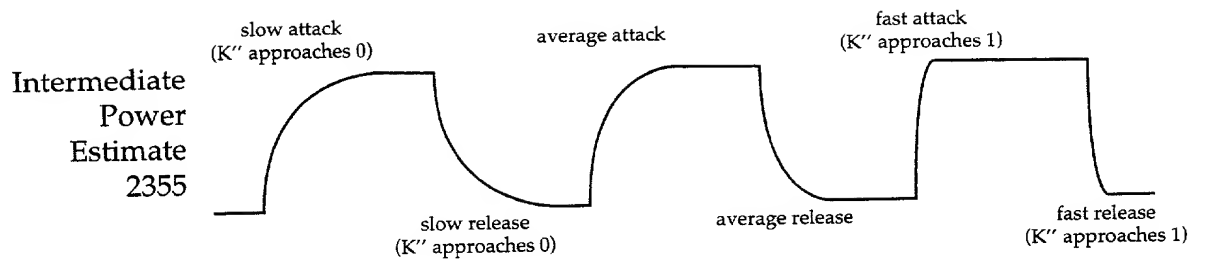


FIG. 24G

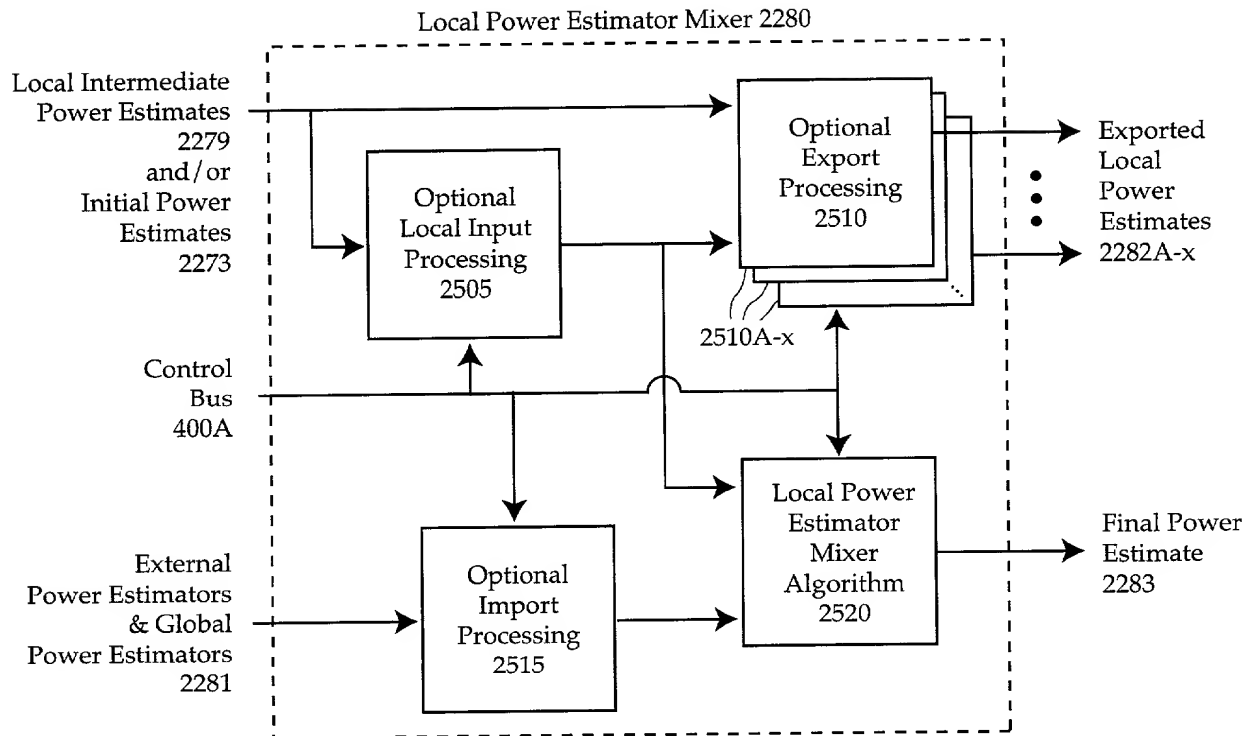


FIG. 25A

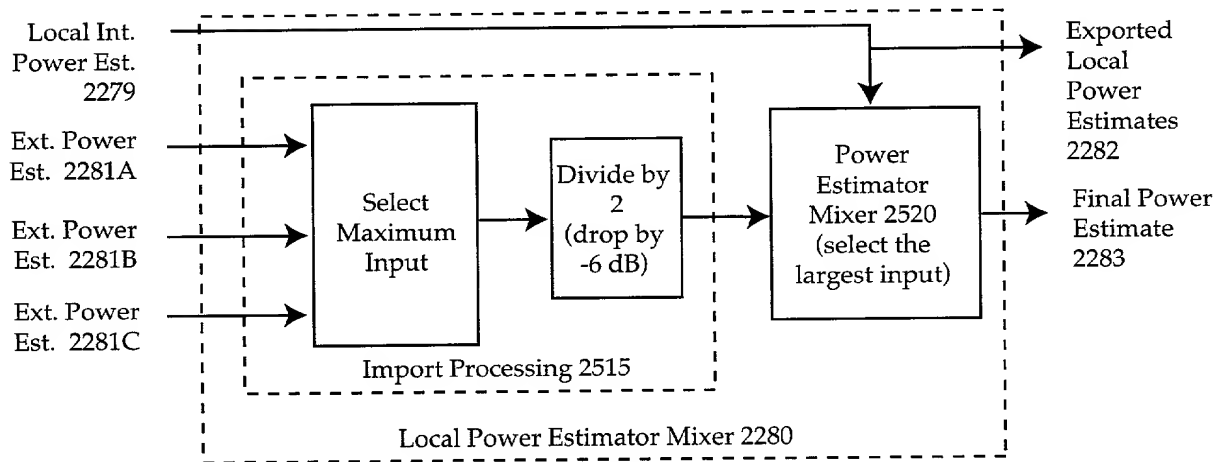


FIG. 25B

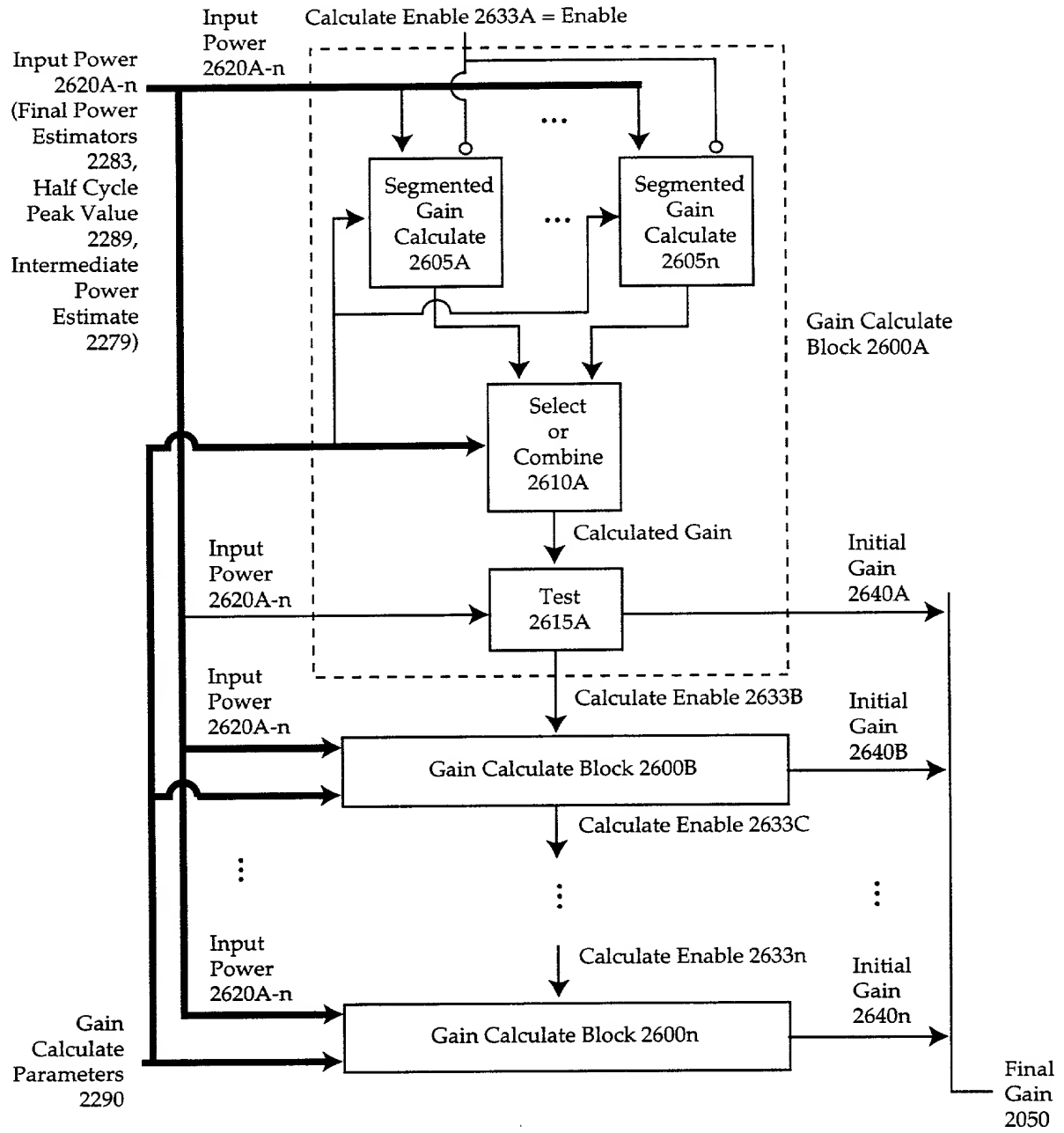


FIG. 26A

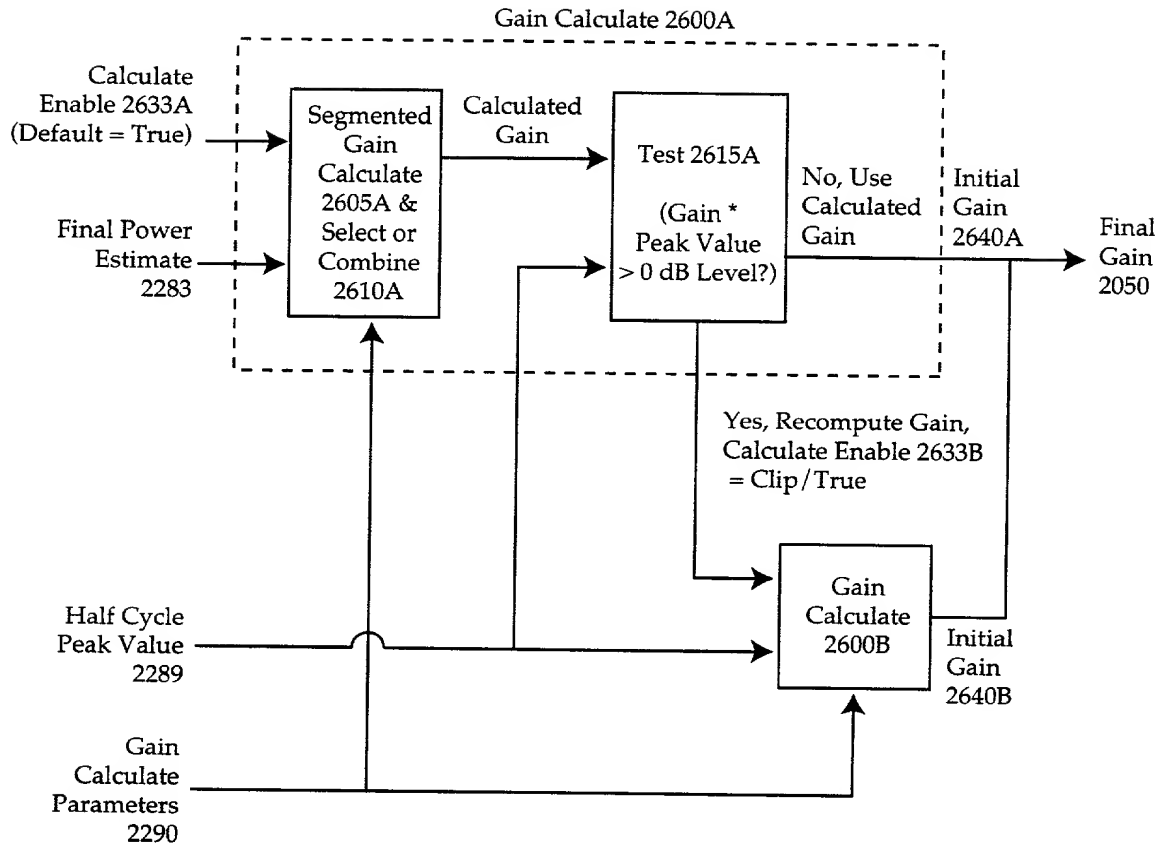


FIG. 26B

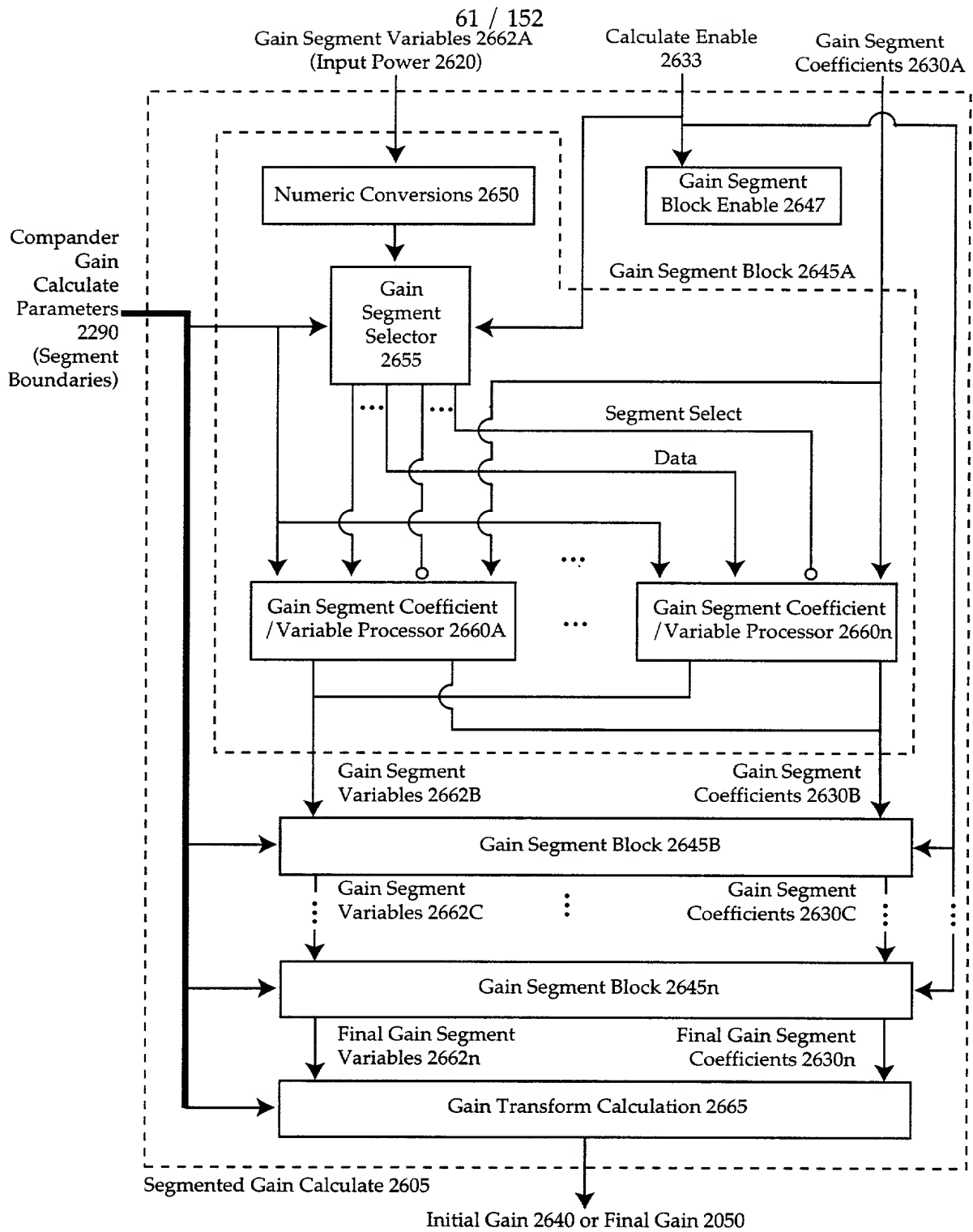


FIG. 26C

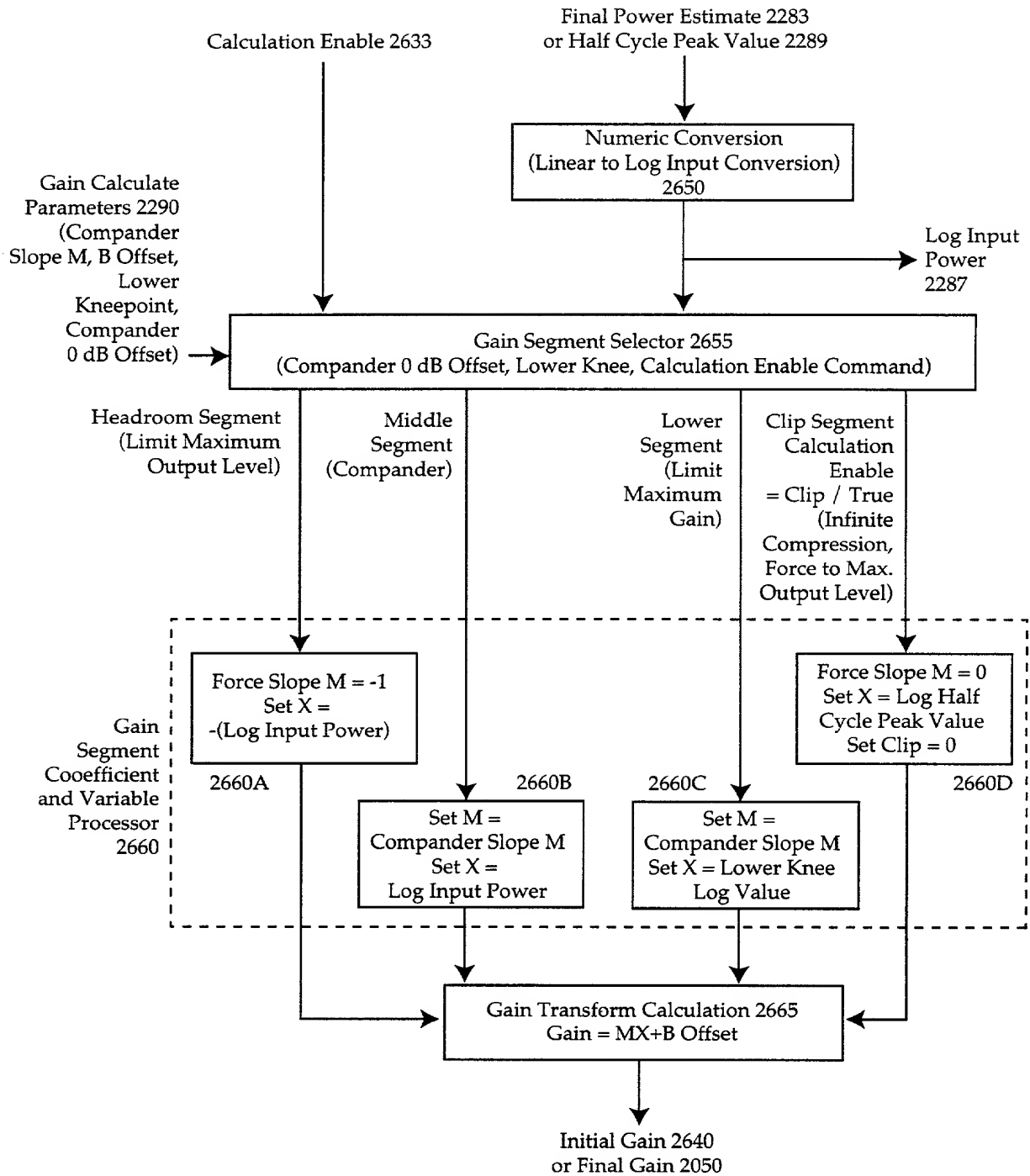


FIG. 26D

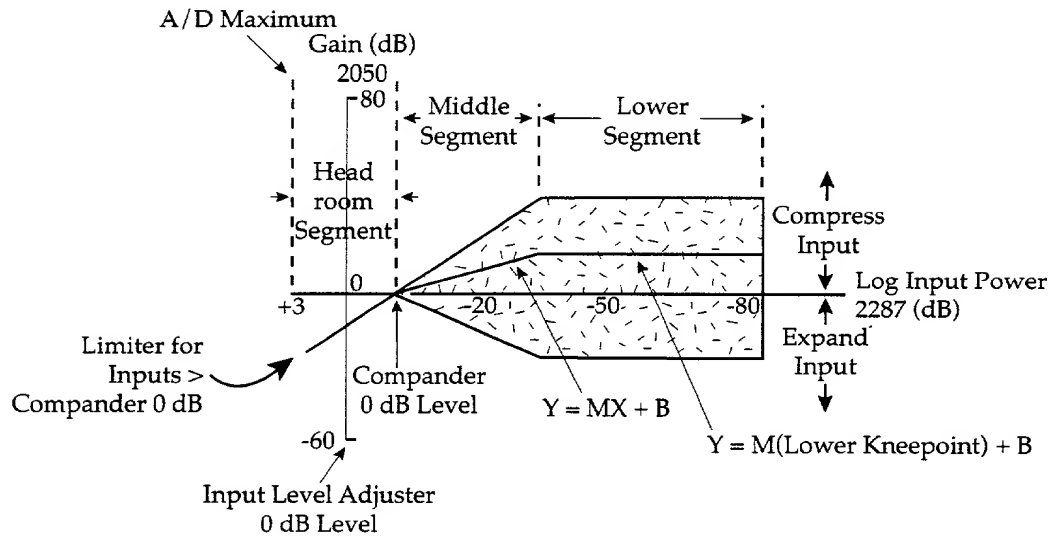


FIG. 26E

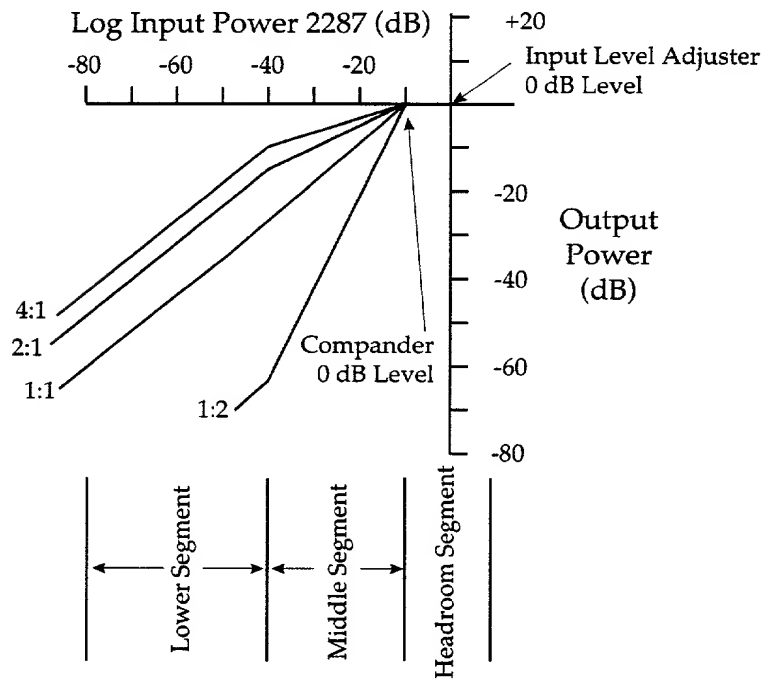


FIG. 26F

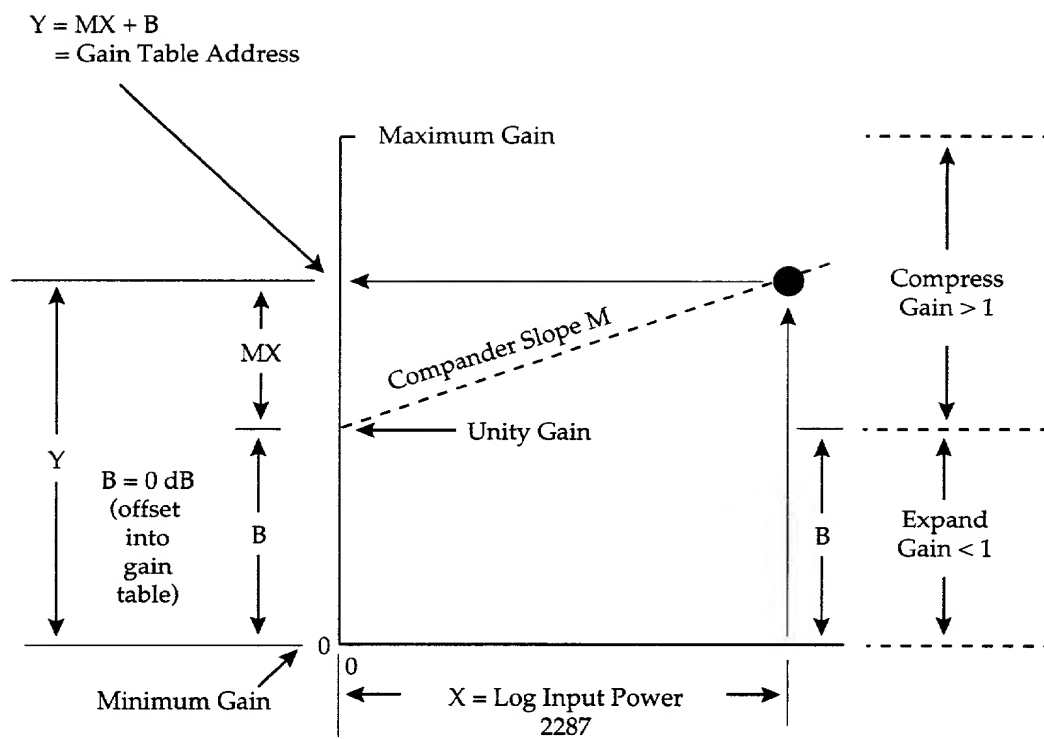


FIG. 26G

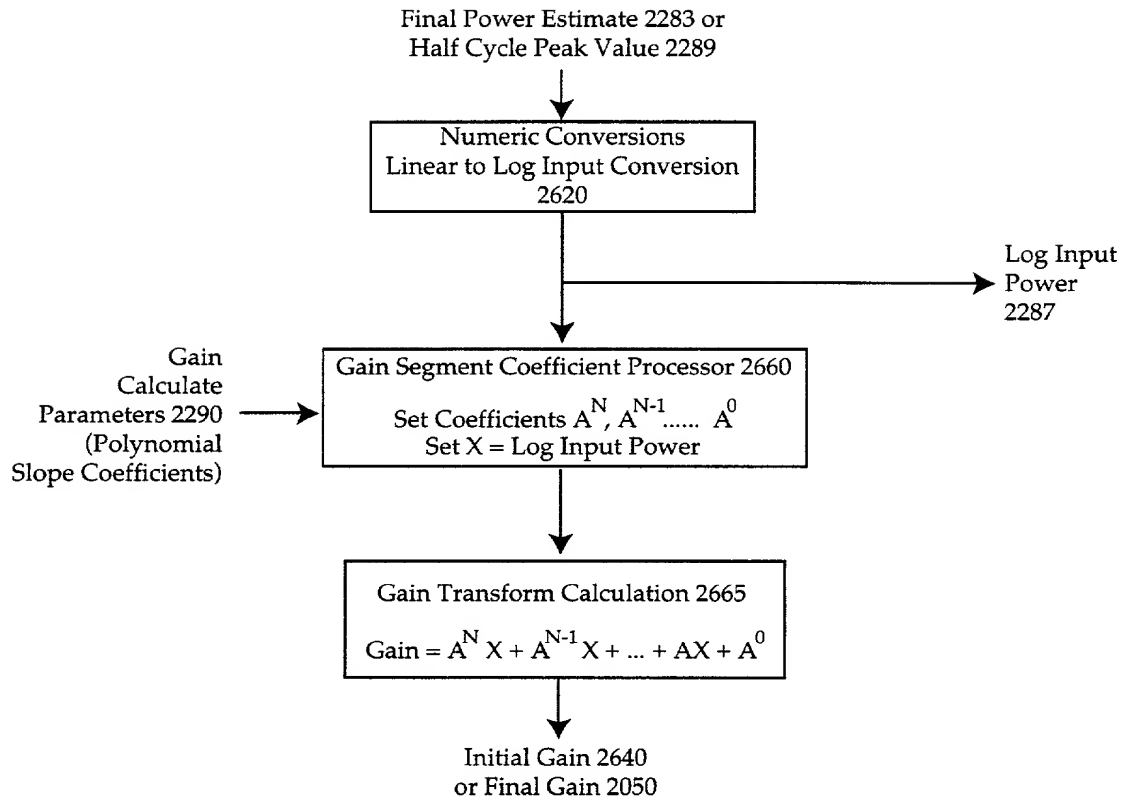


FIG. 26H

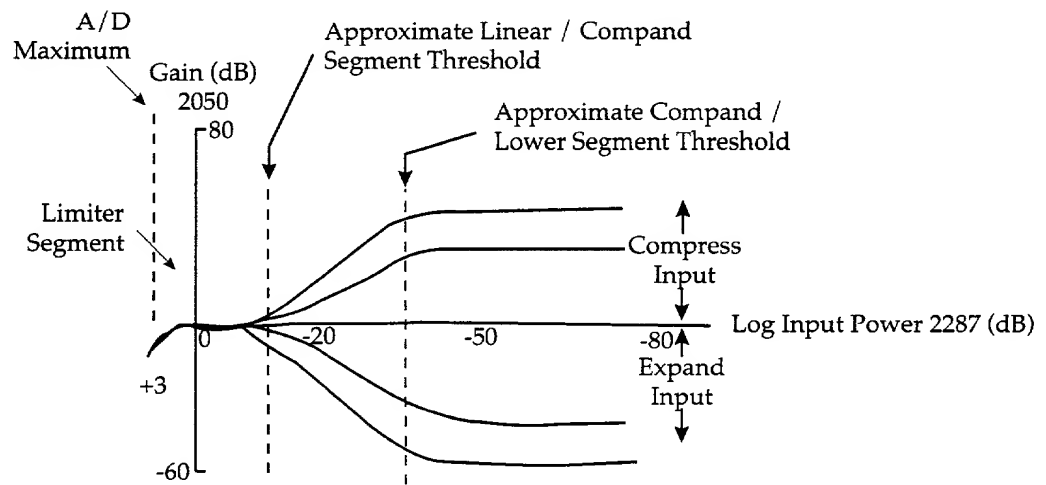


FIG. 26I

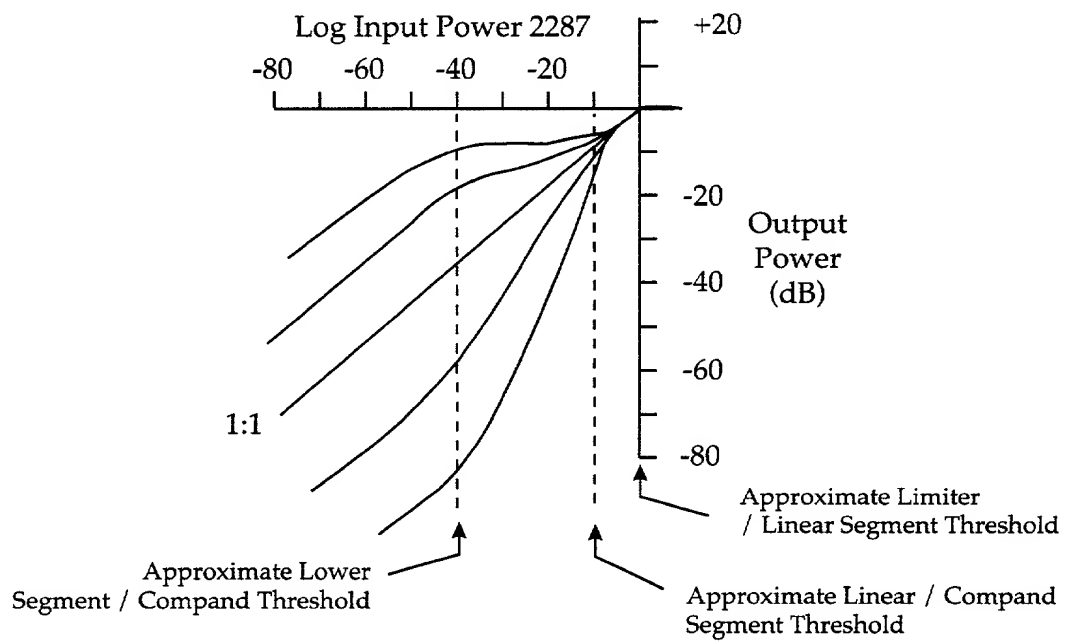


FIG. 26J

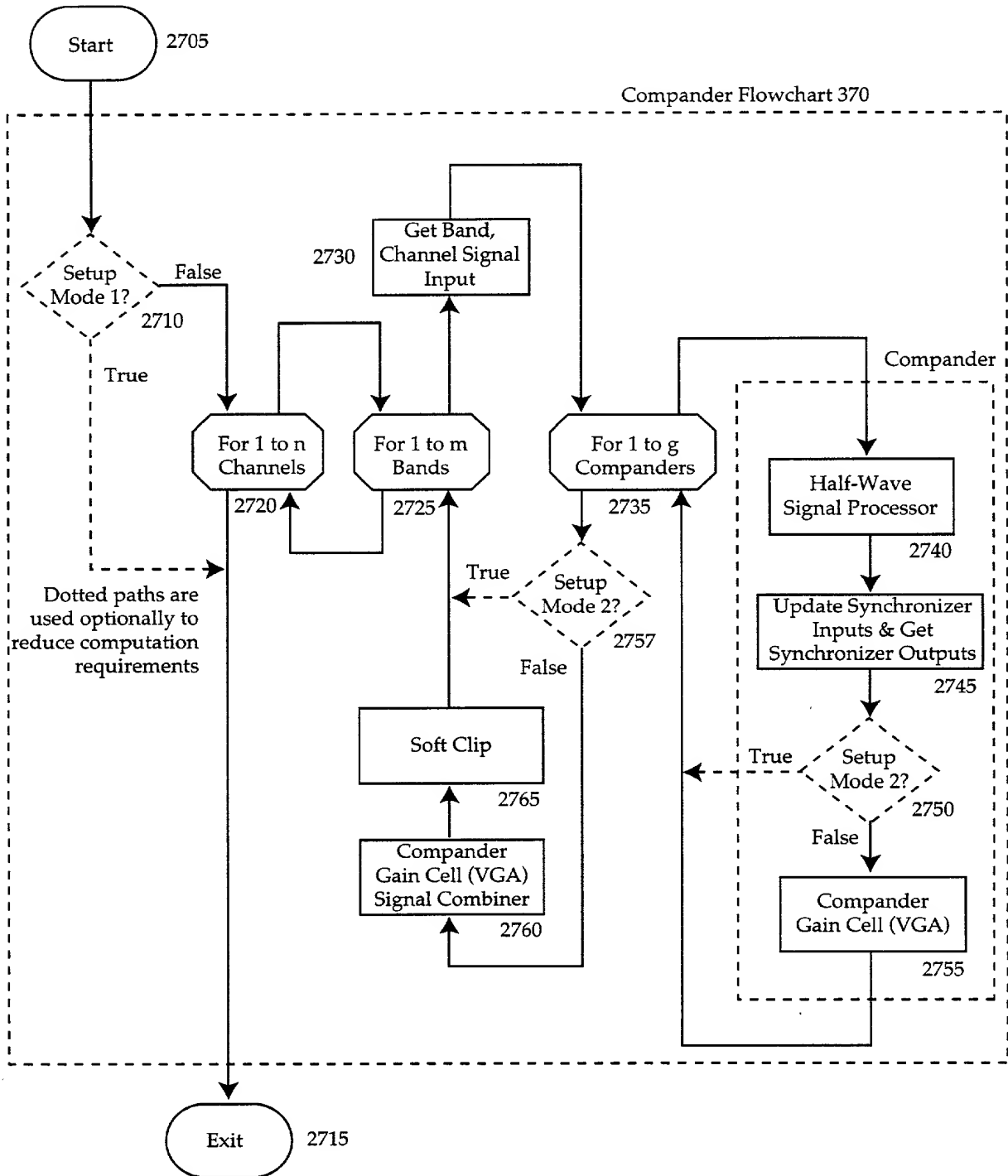


FIG. 27A

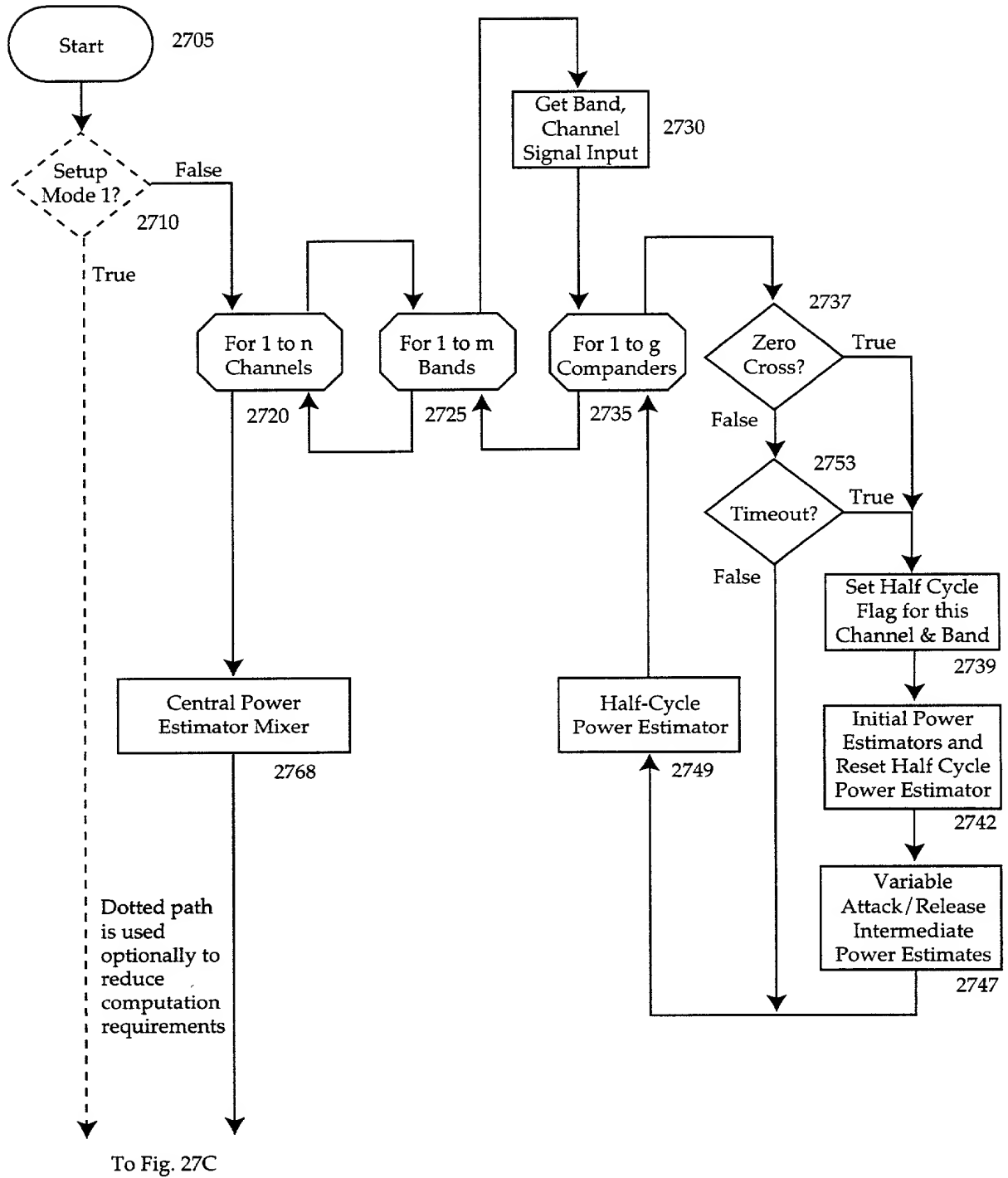


FIG. 27B

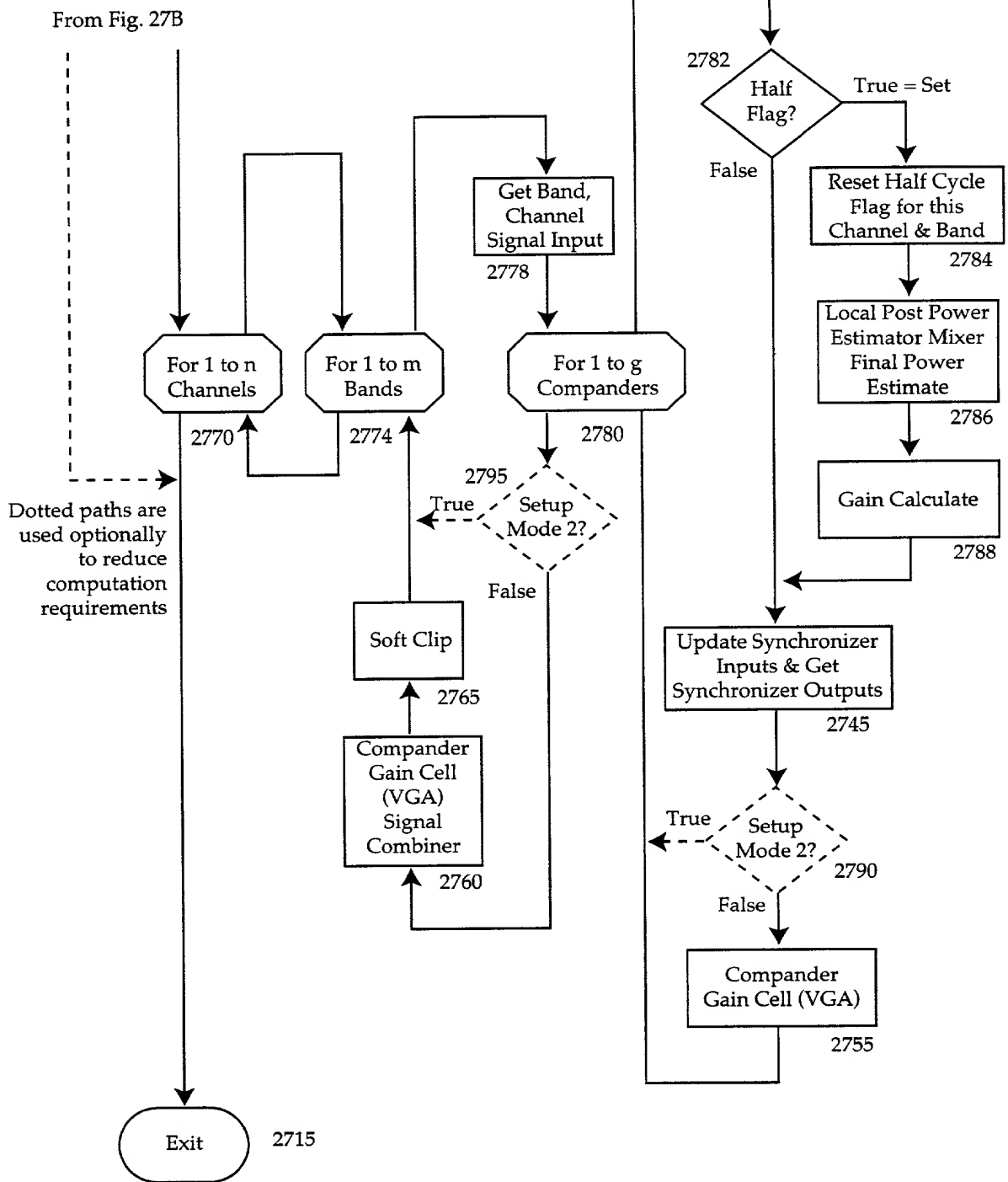


FIG. 27C

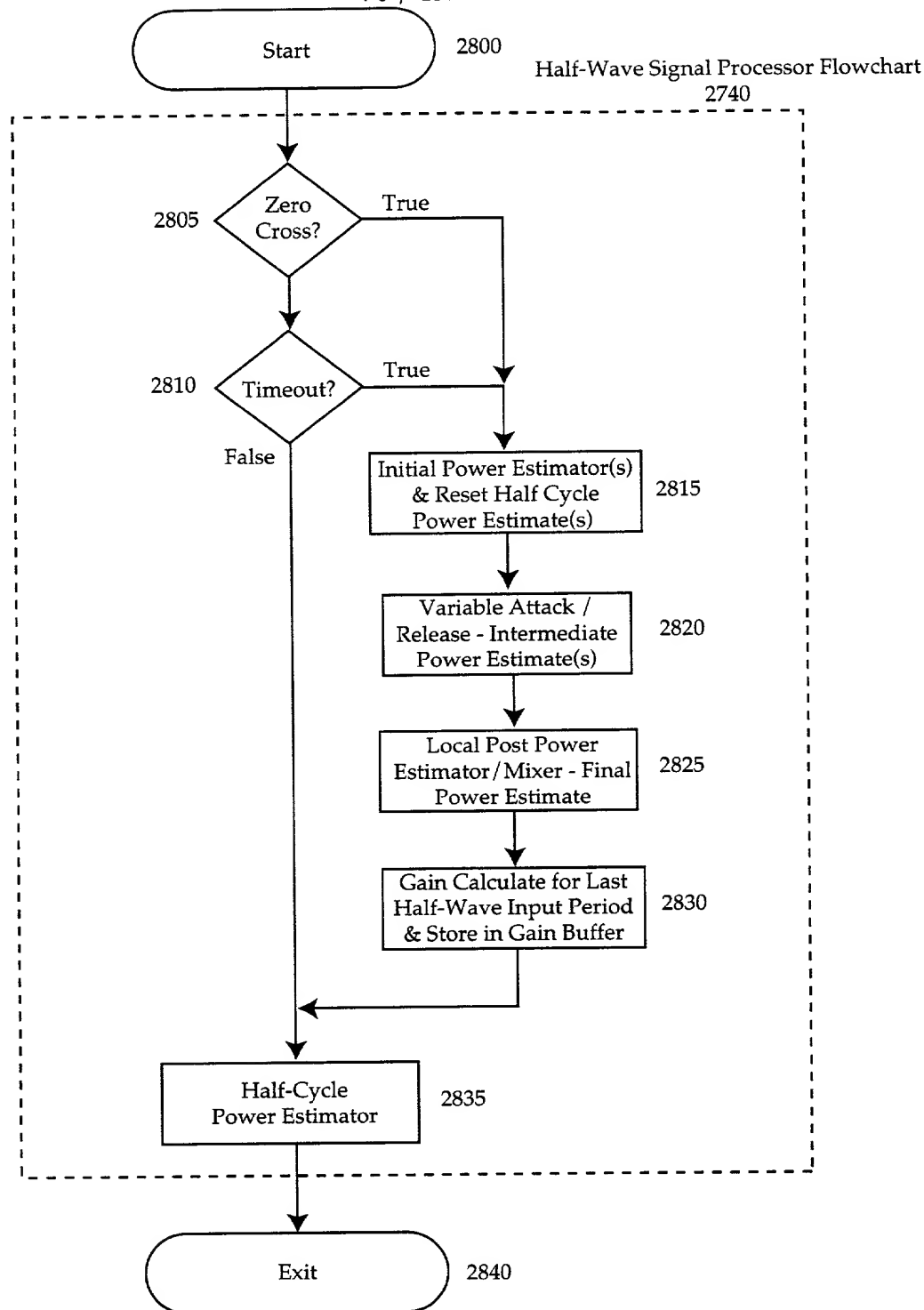


FIG. 28

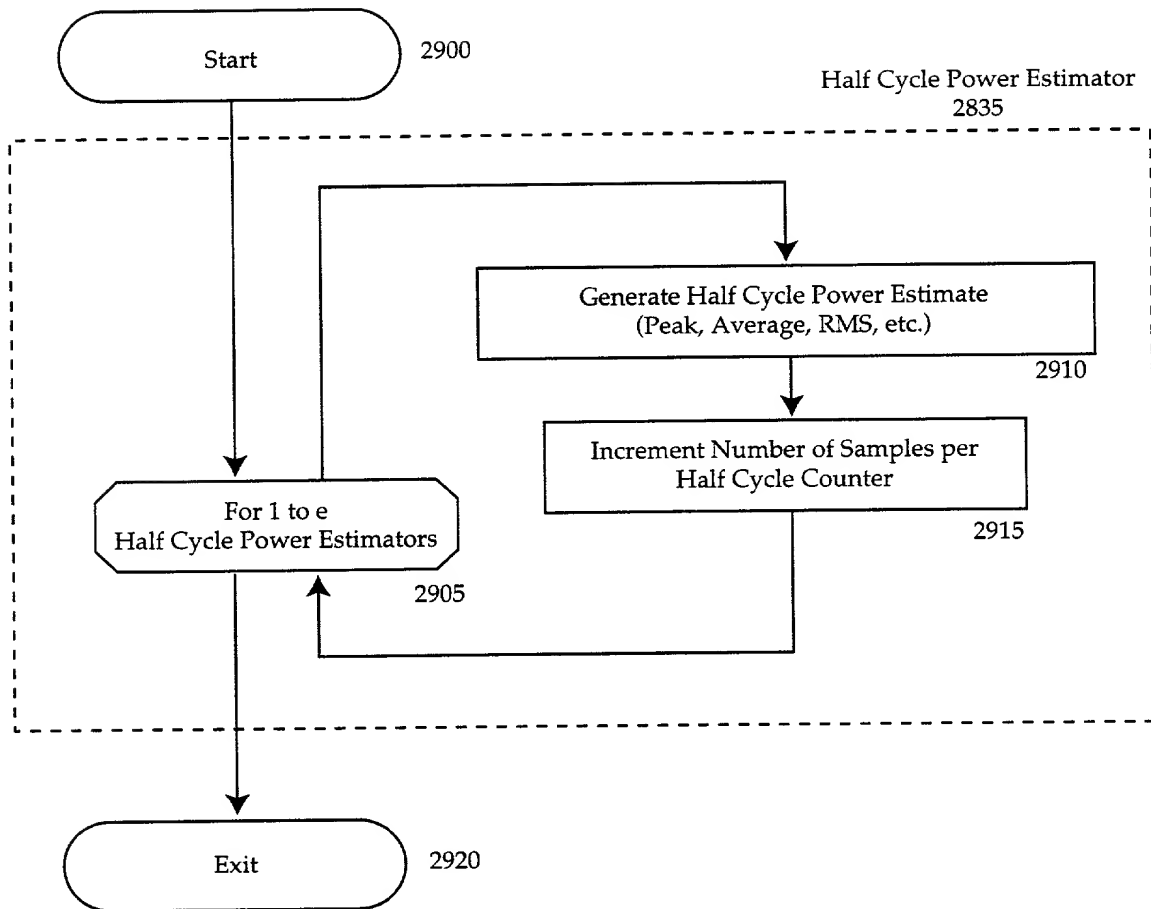


FIG. 29

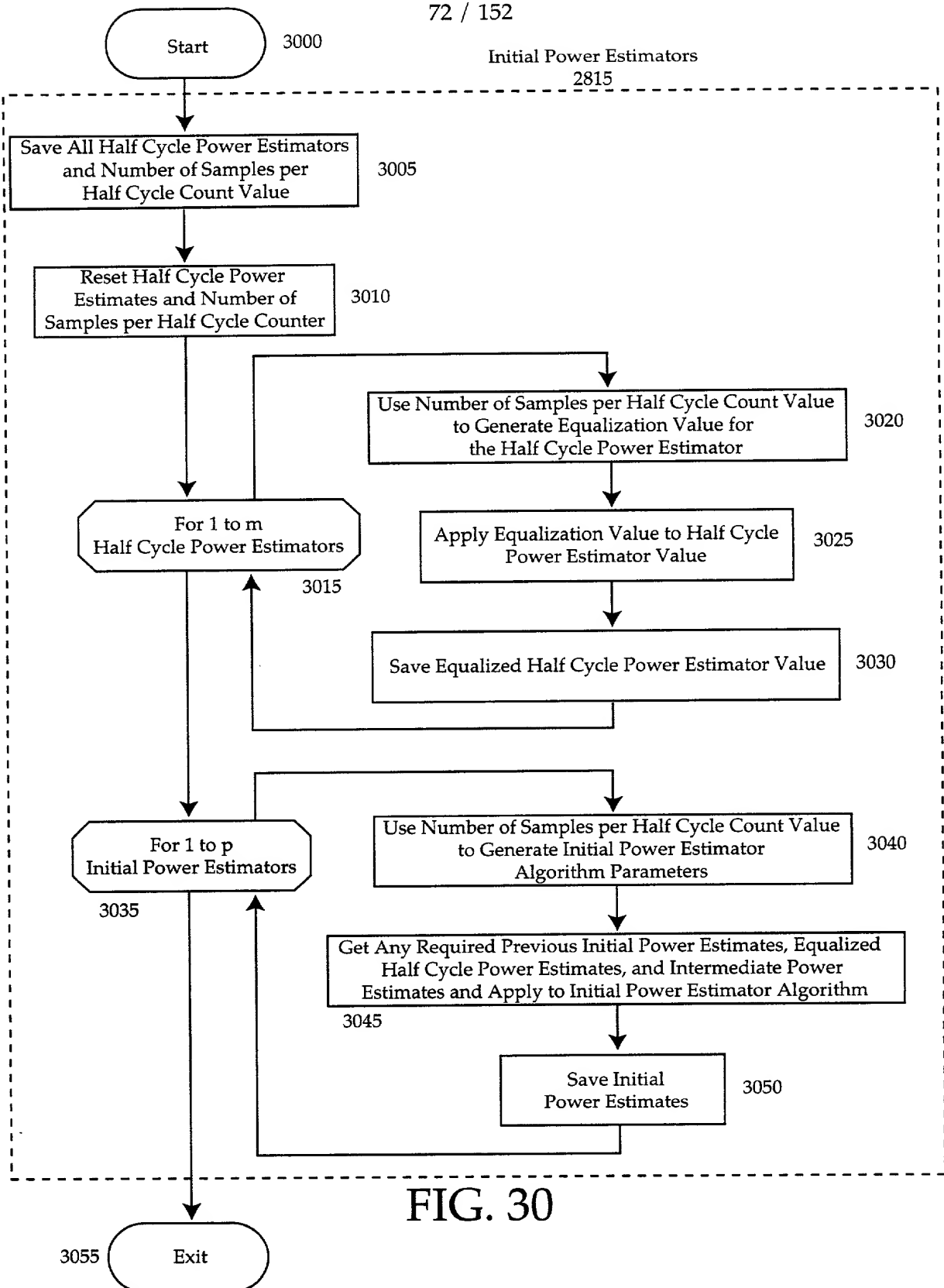


FIG. 30

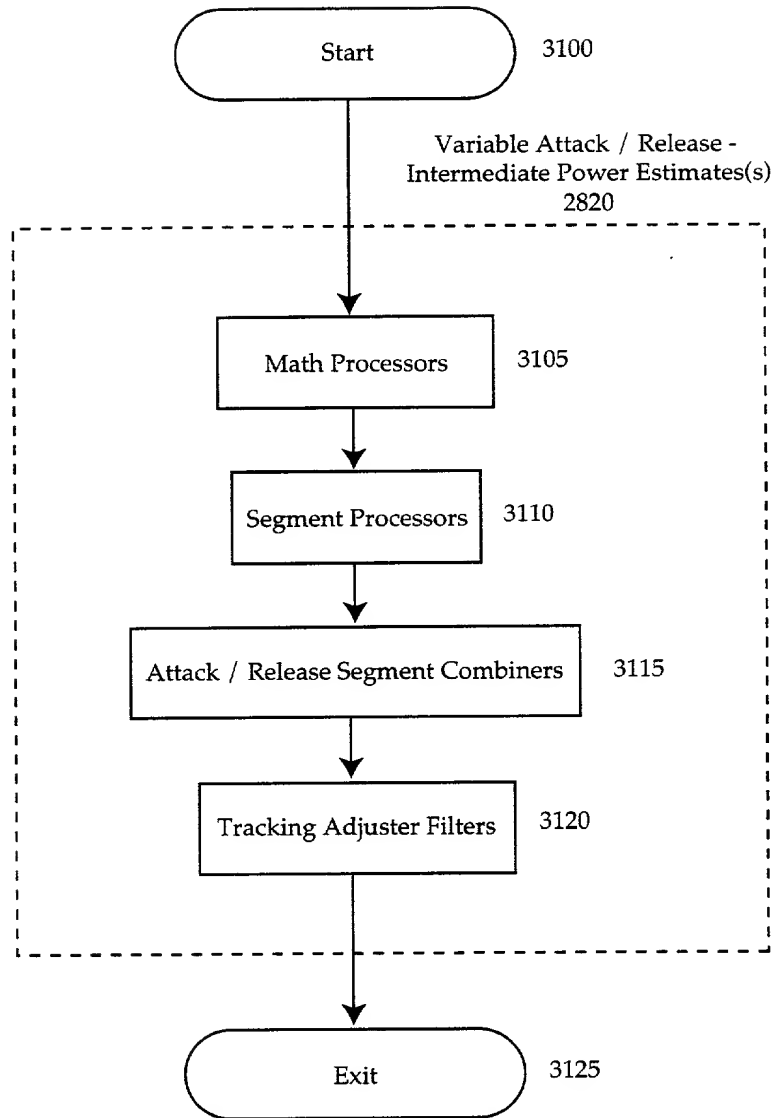


FIG. 31

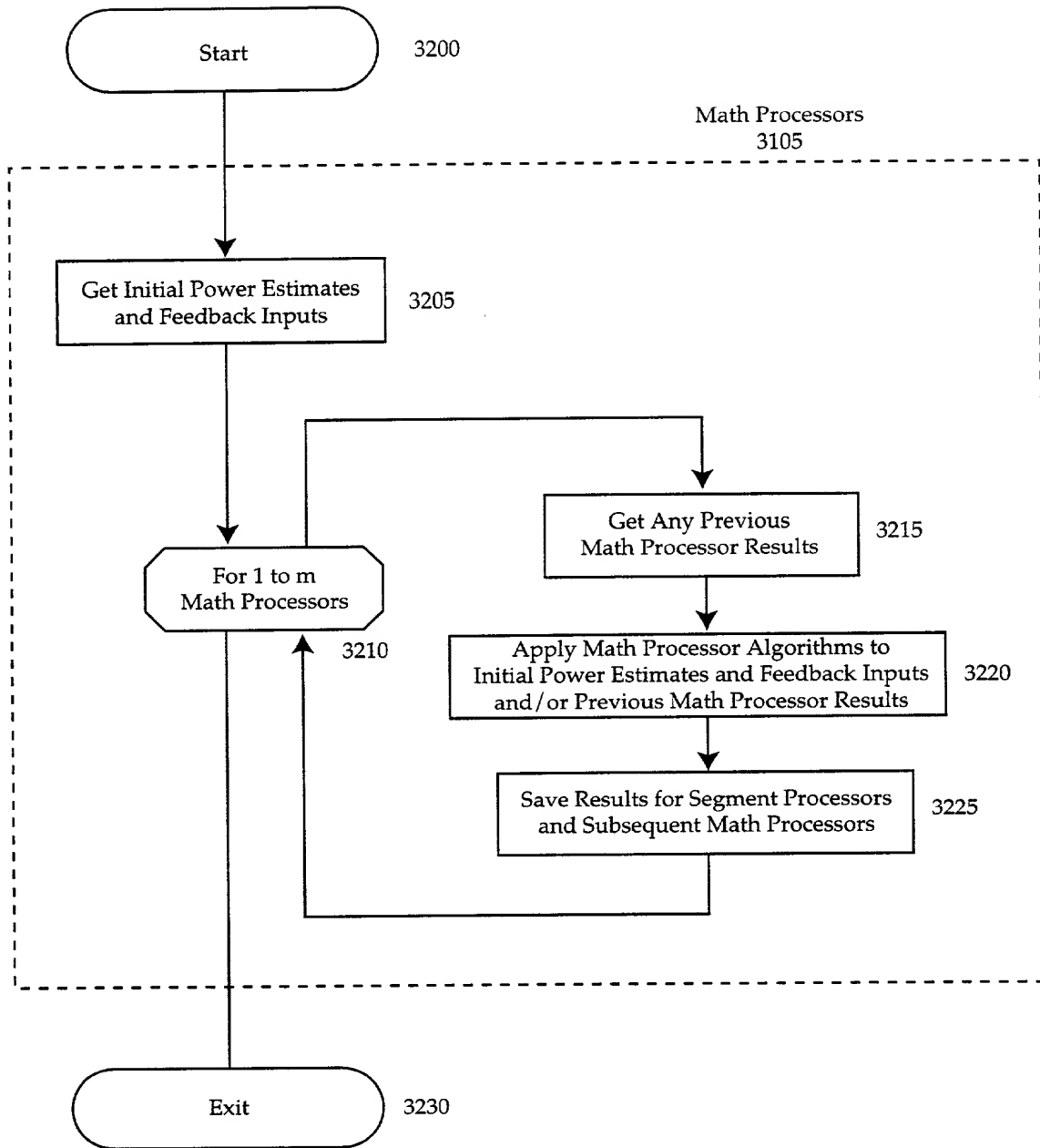


FIG. 32

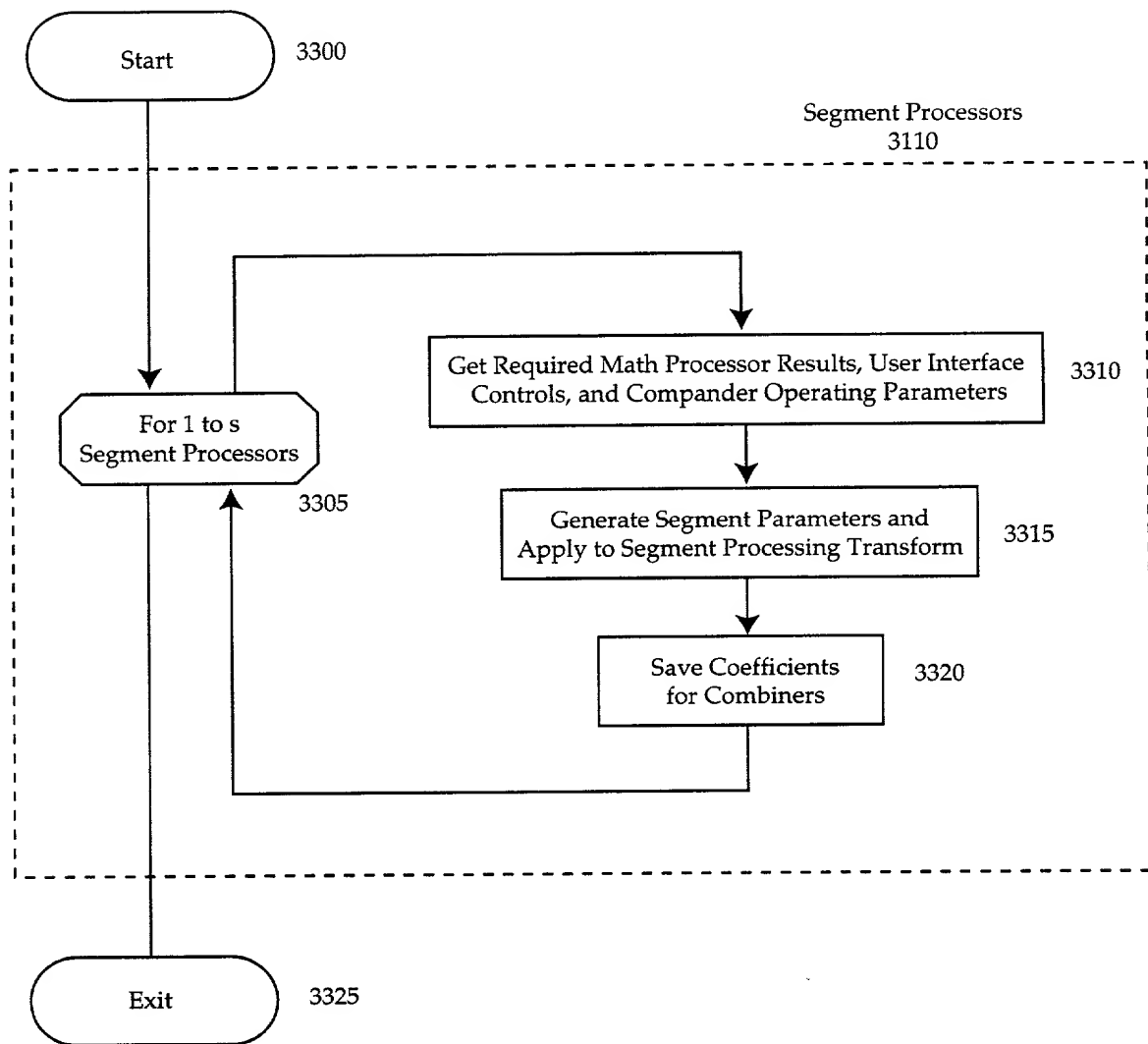


FIG. 33

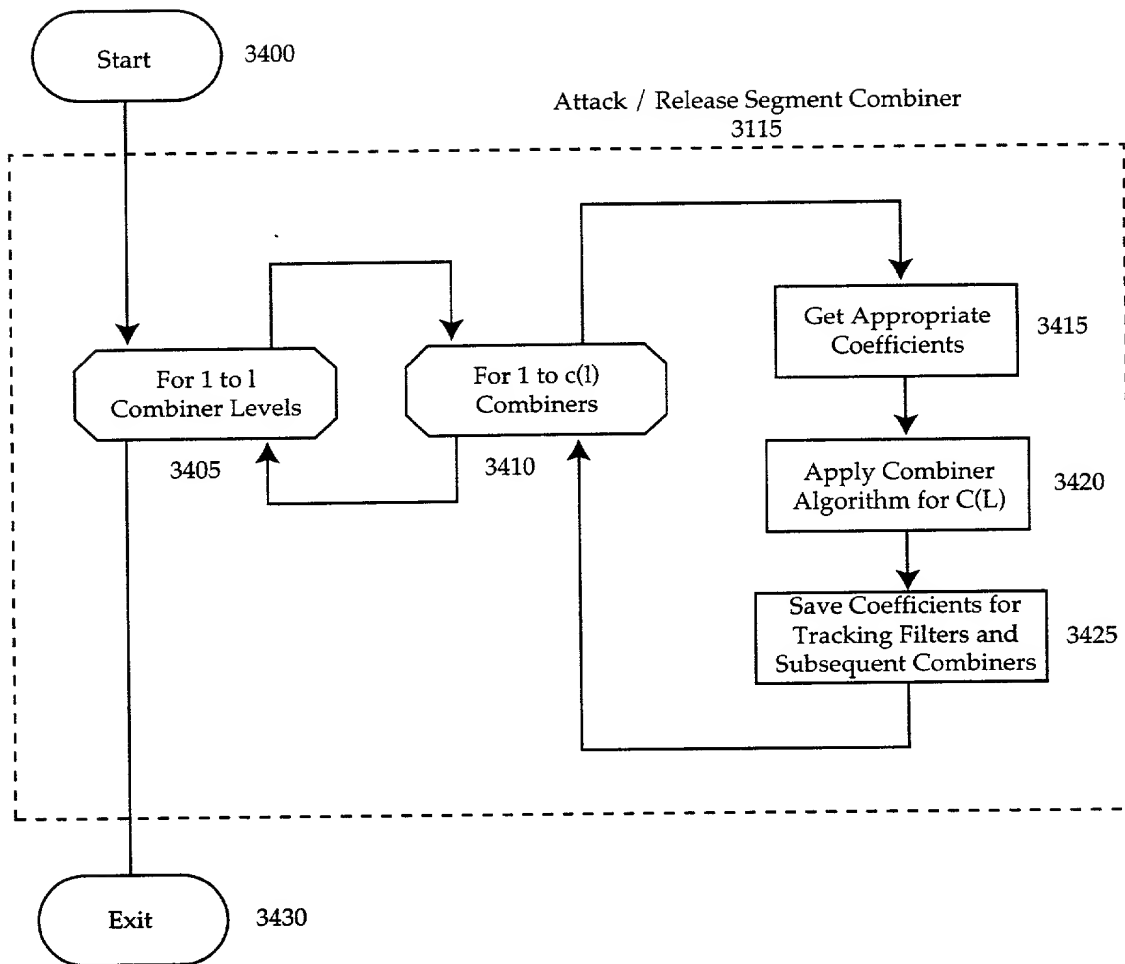


FIG. 34

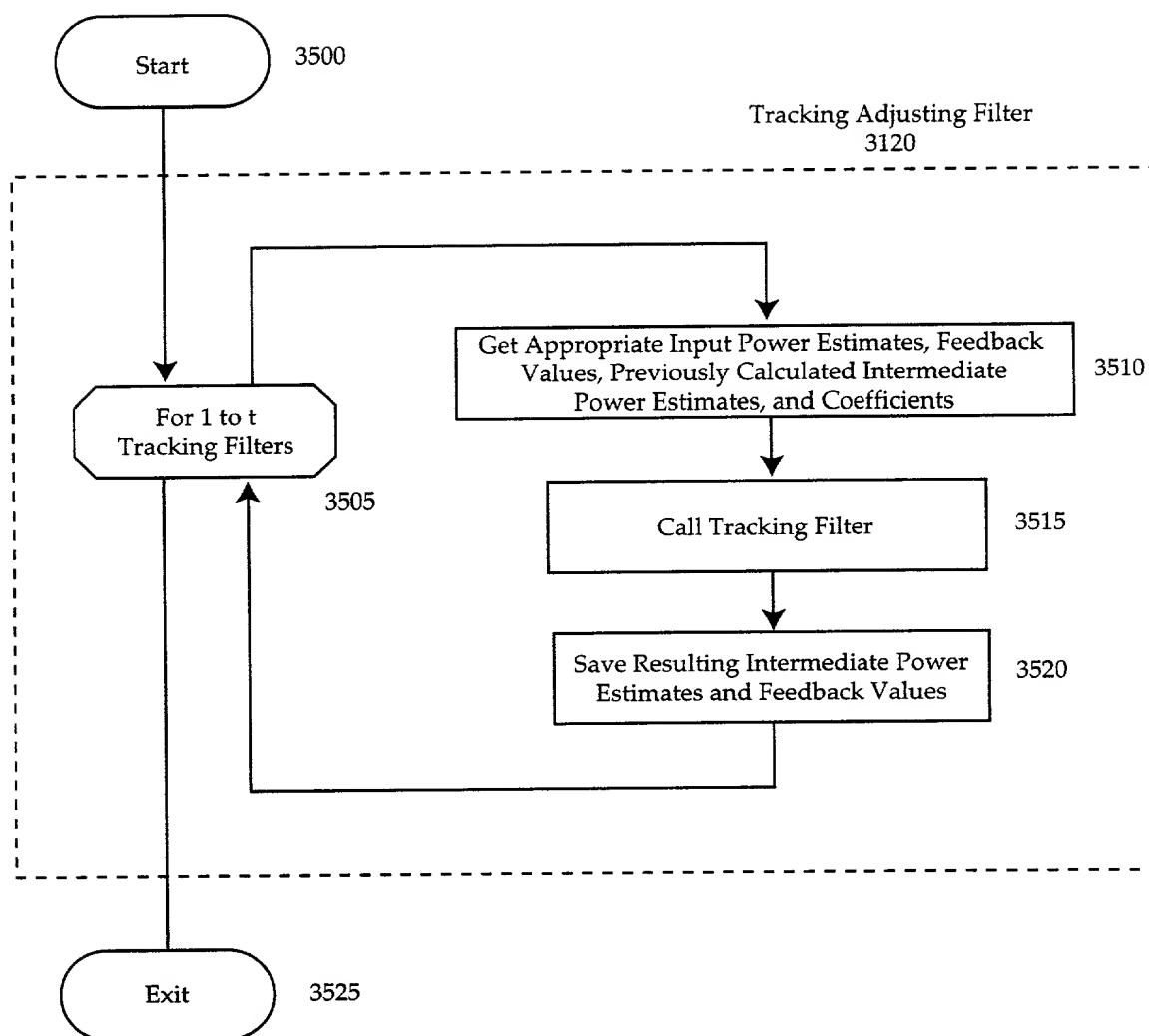


FIG. 35

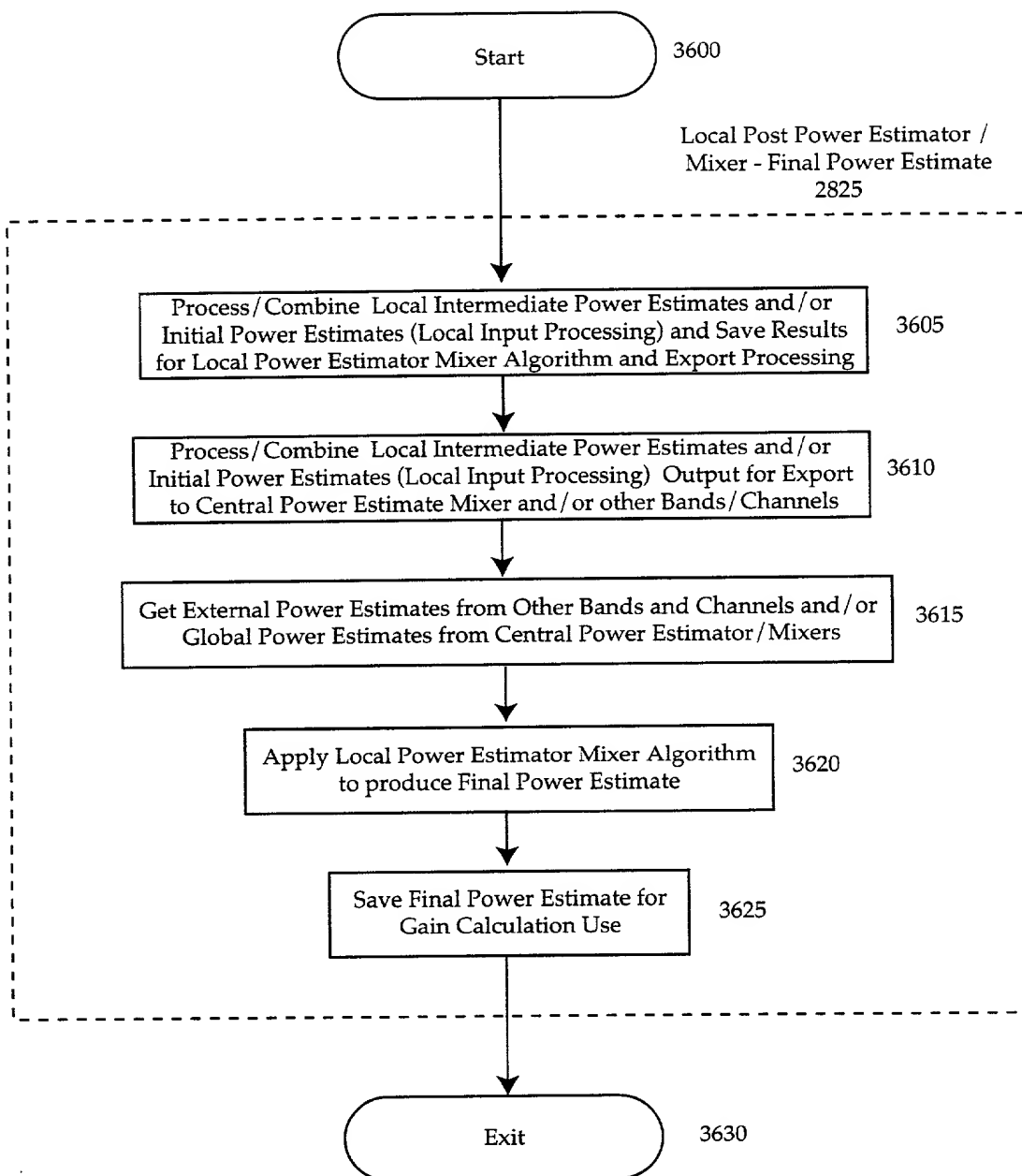


FIG. 36

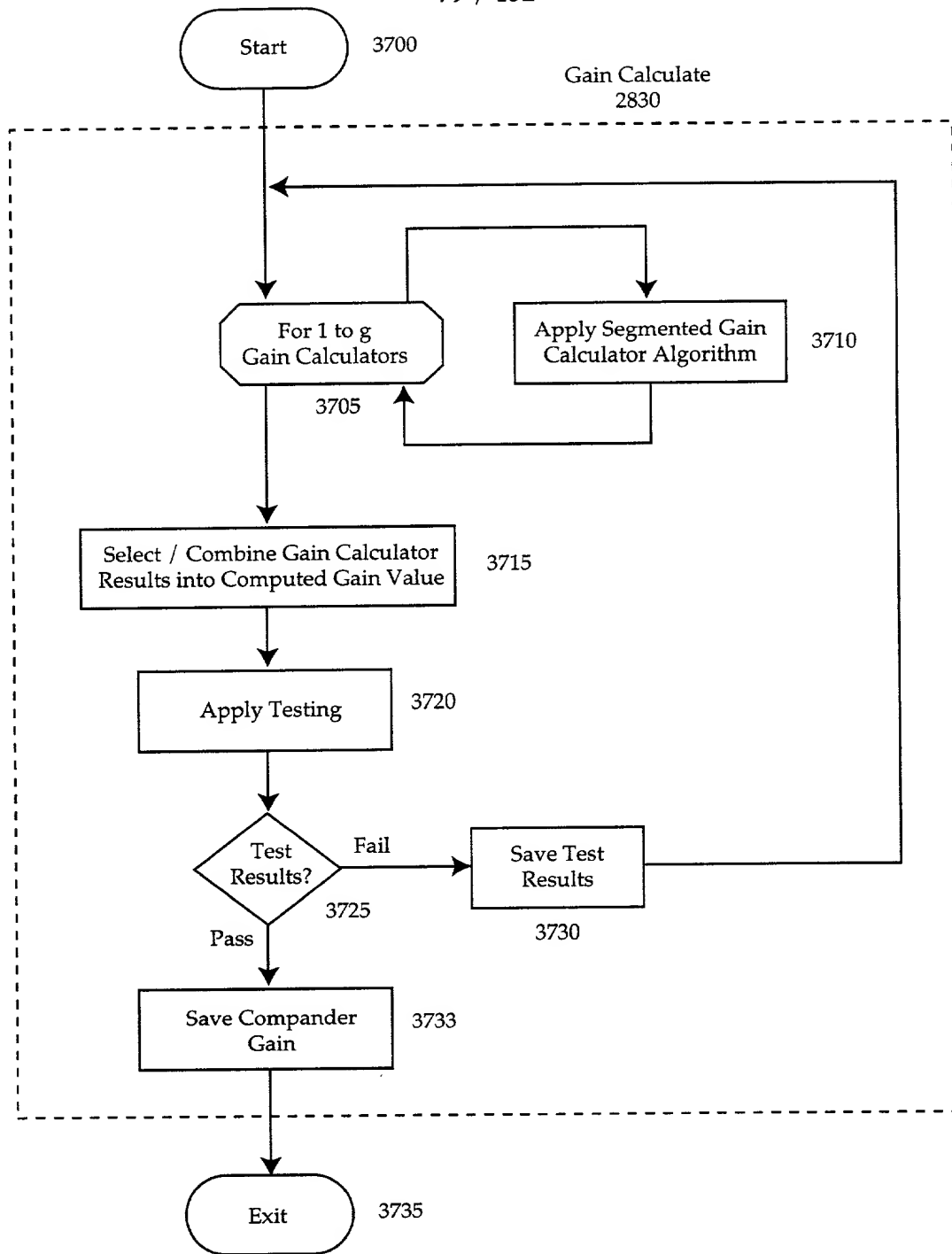


FIG. 37A

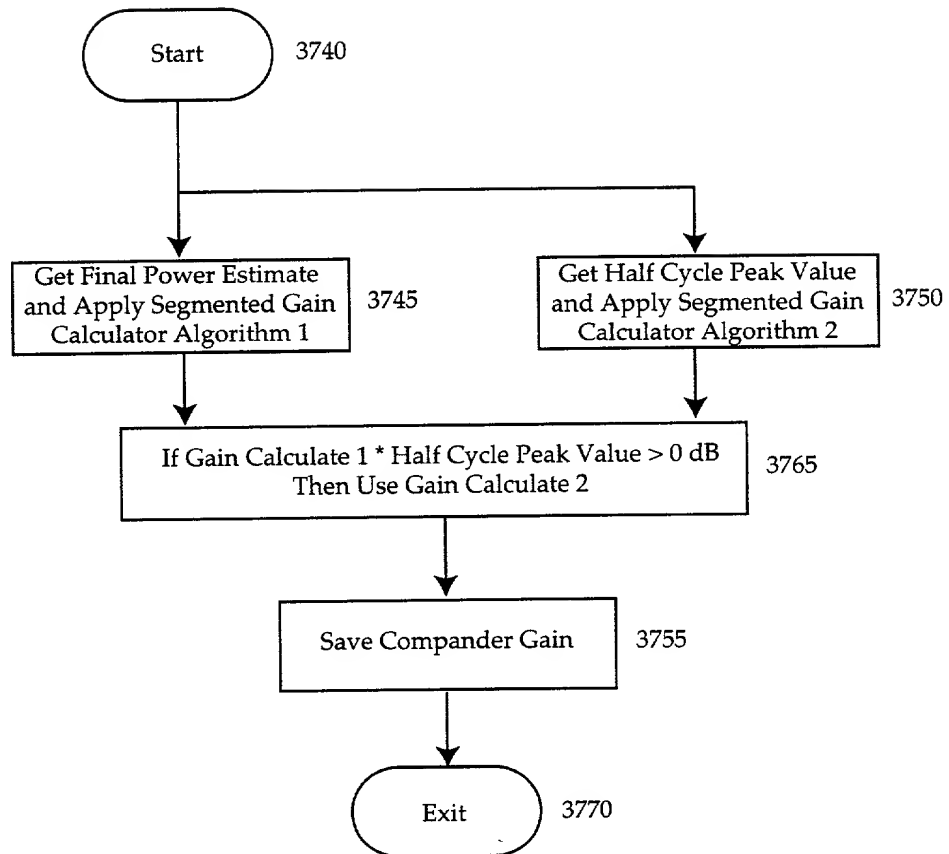


FIG. 37B

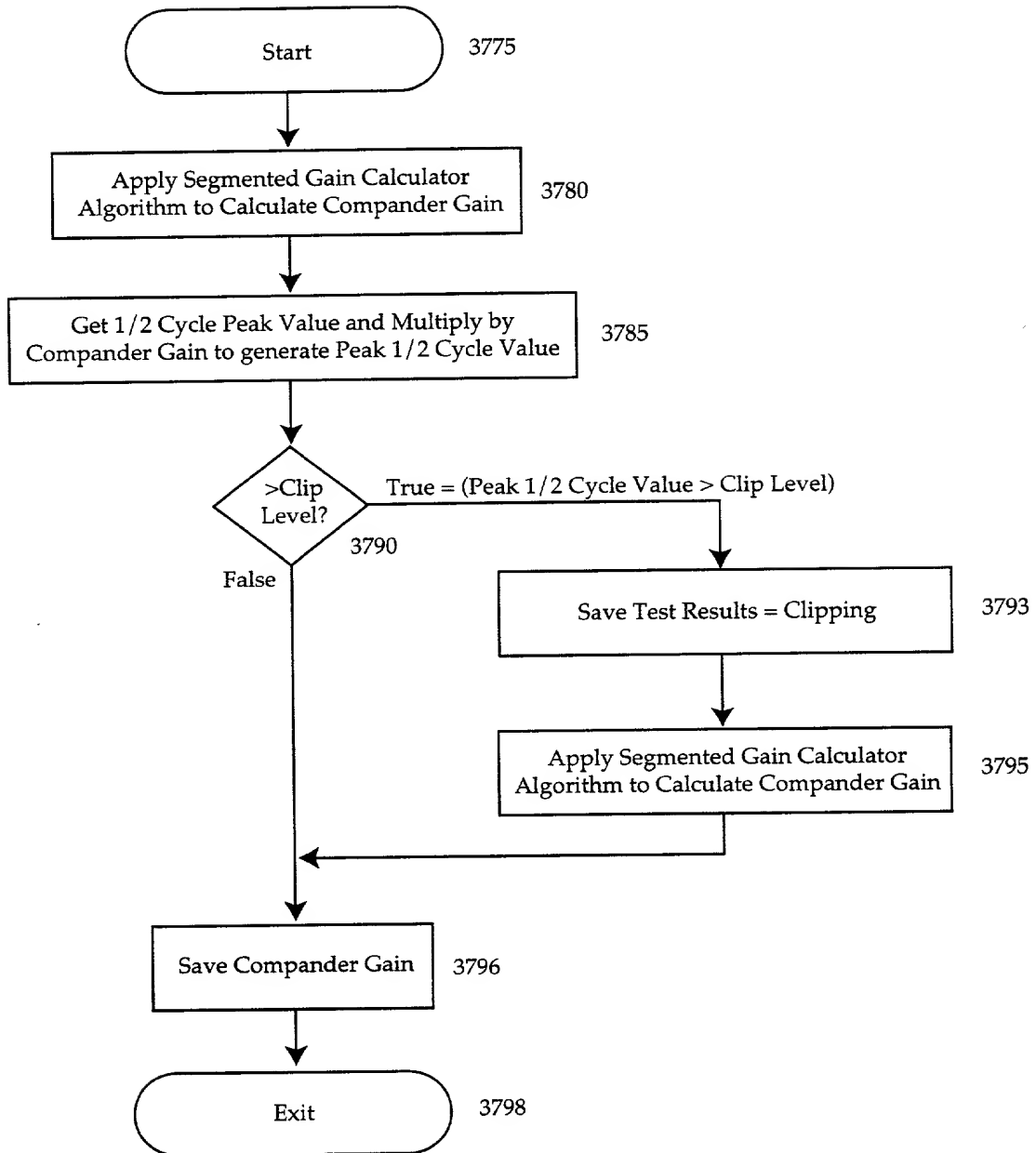


FIG. 37C

3800

Start

Segmented Gain Calculate Algorithm
3710, 3755, 3760, 3780, 3795

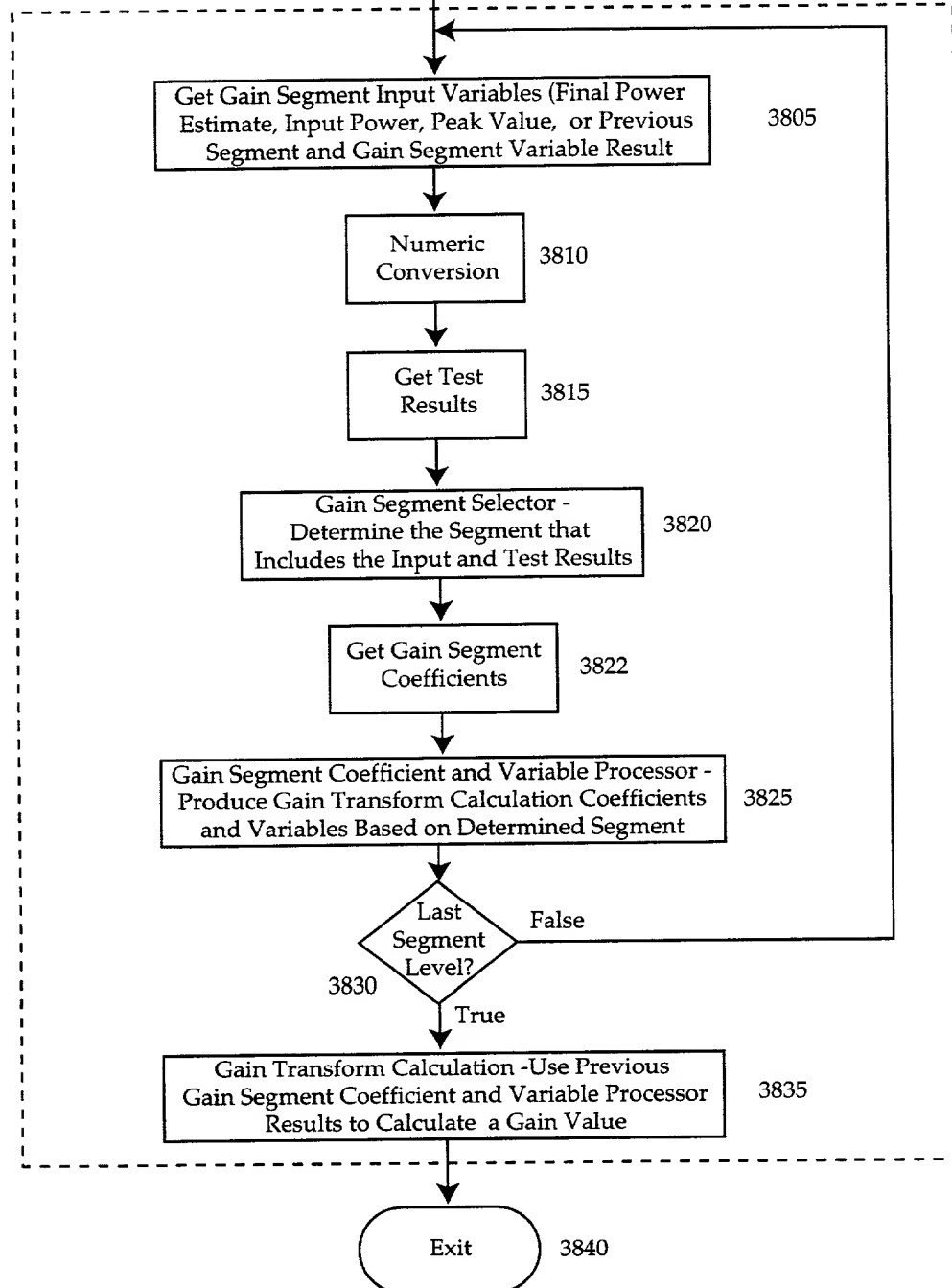


FIG. 38

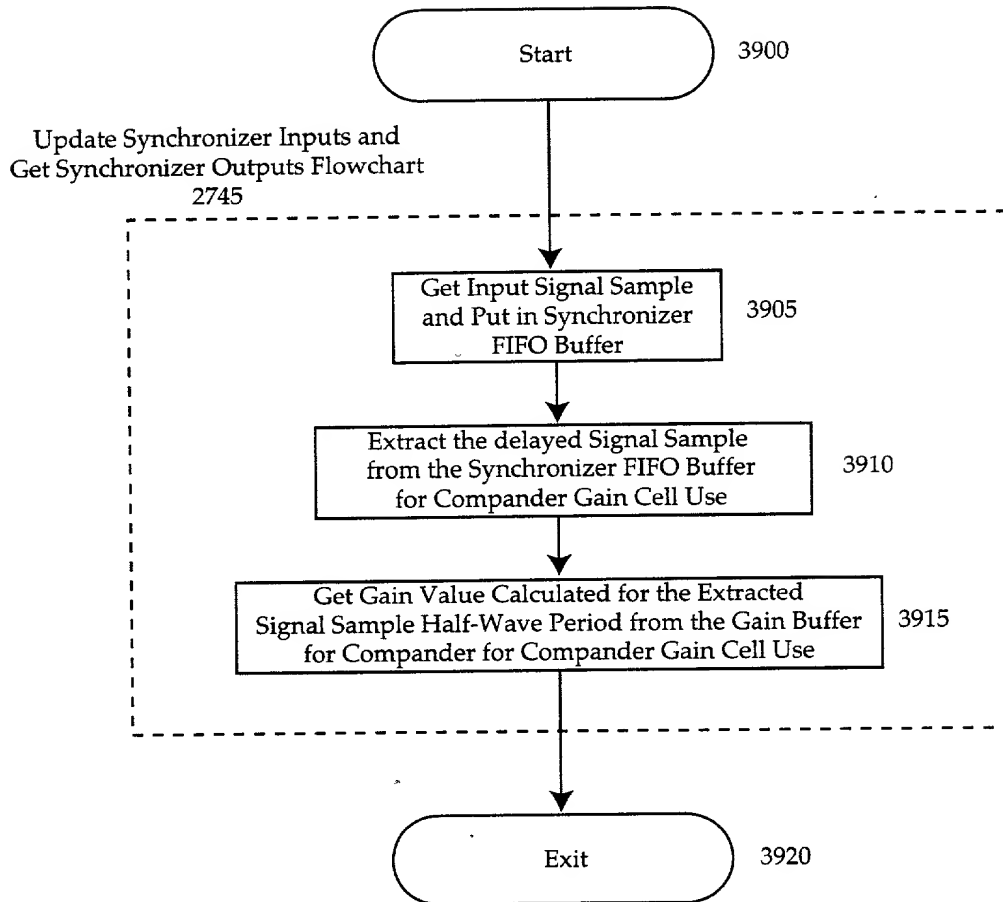
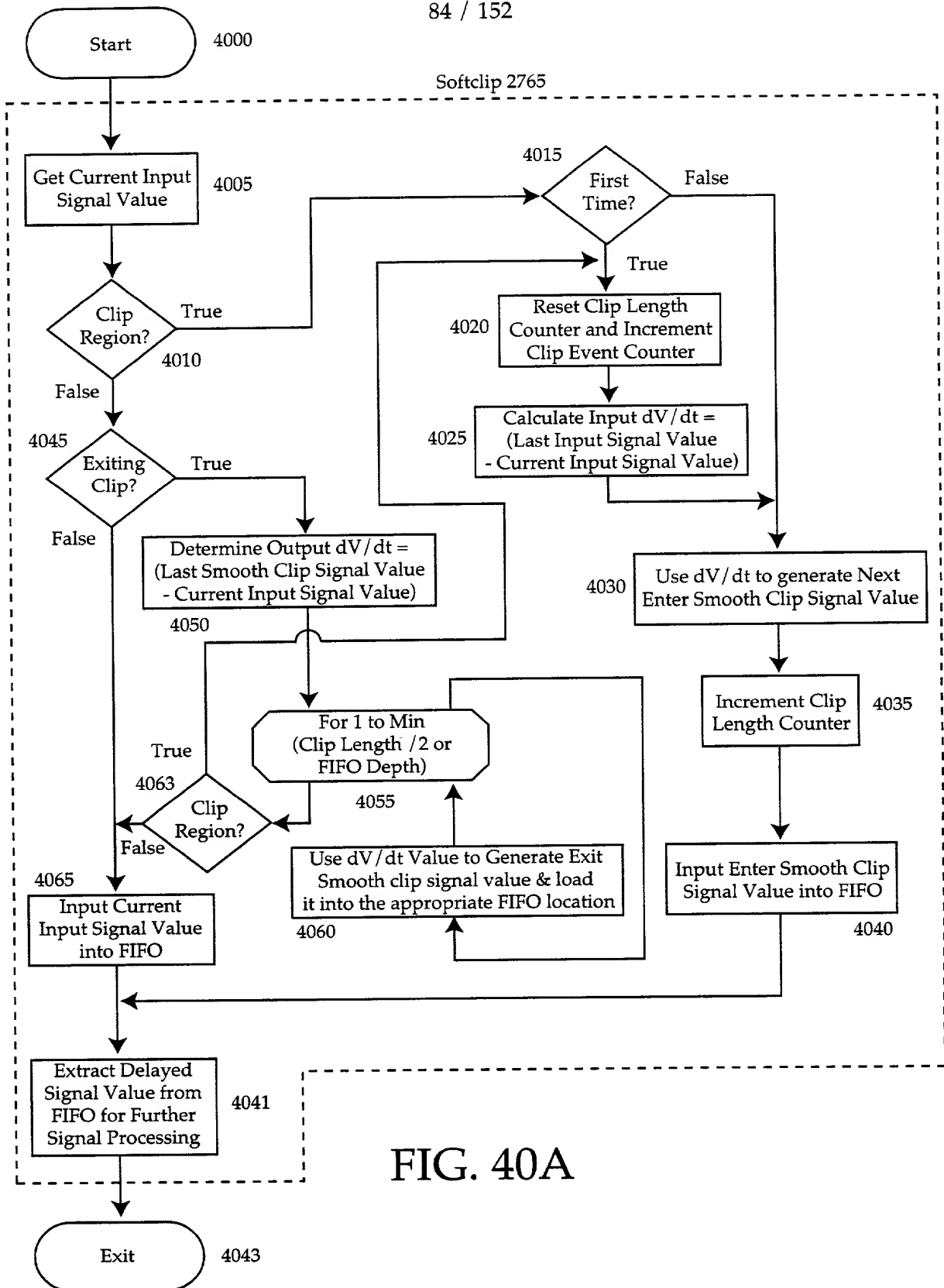


FIG. 39



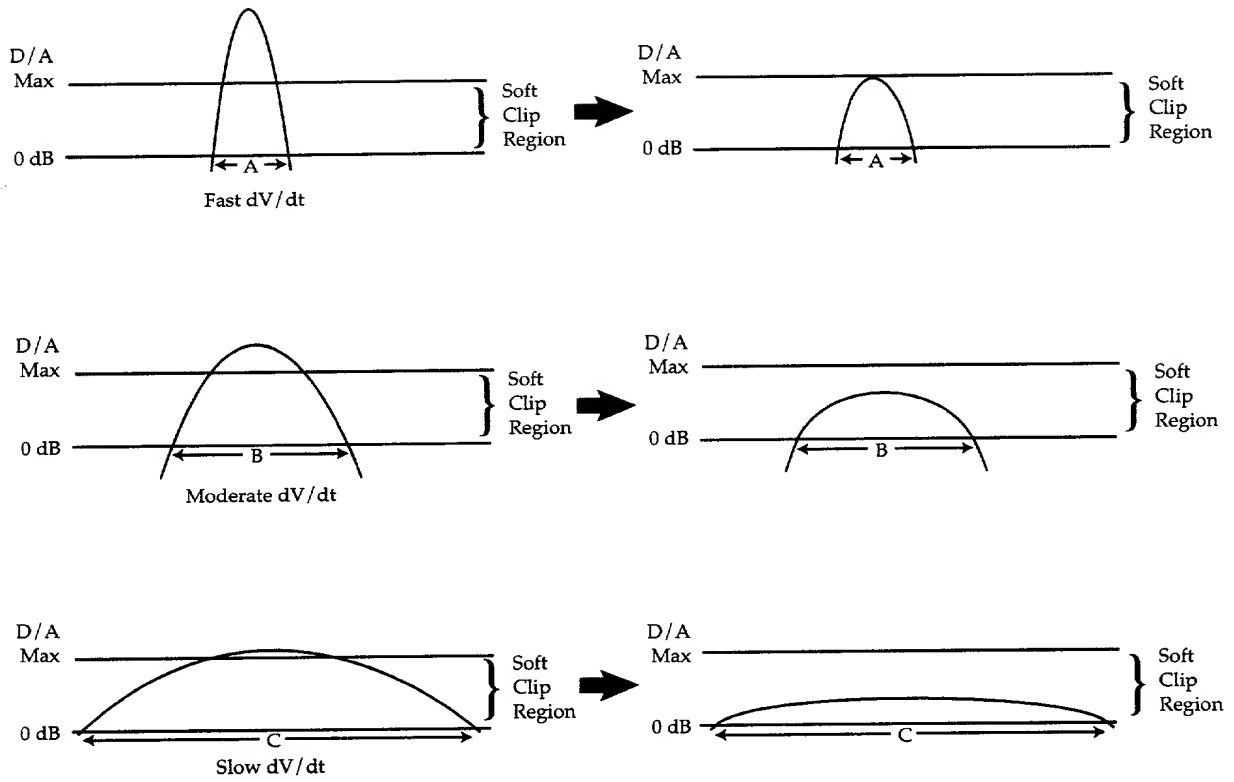


FIG. 40B

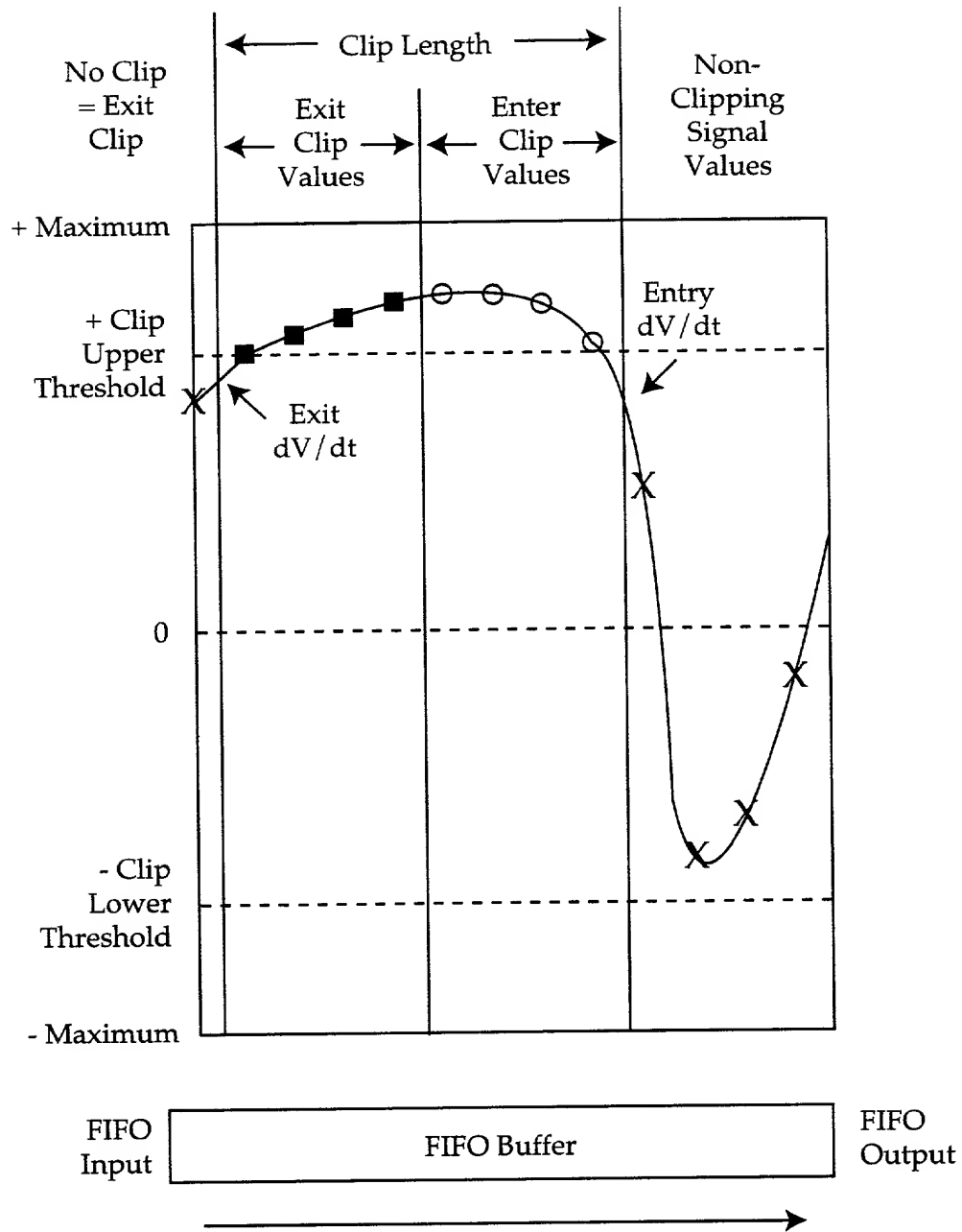


FIG. 40C

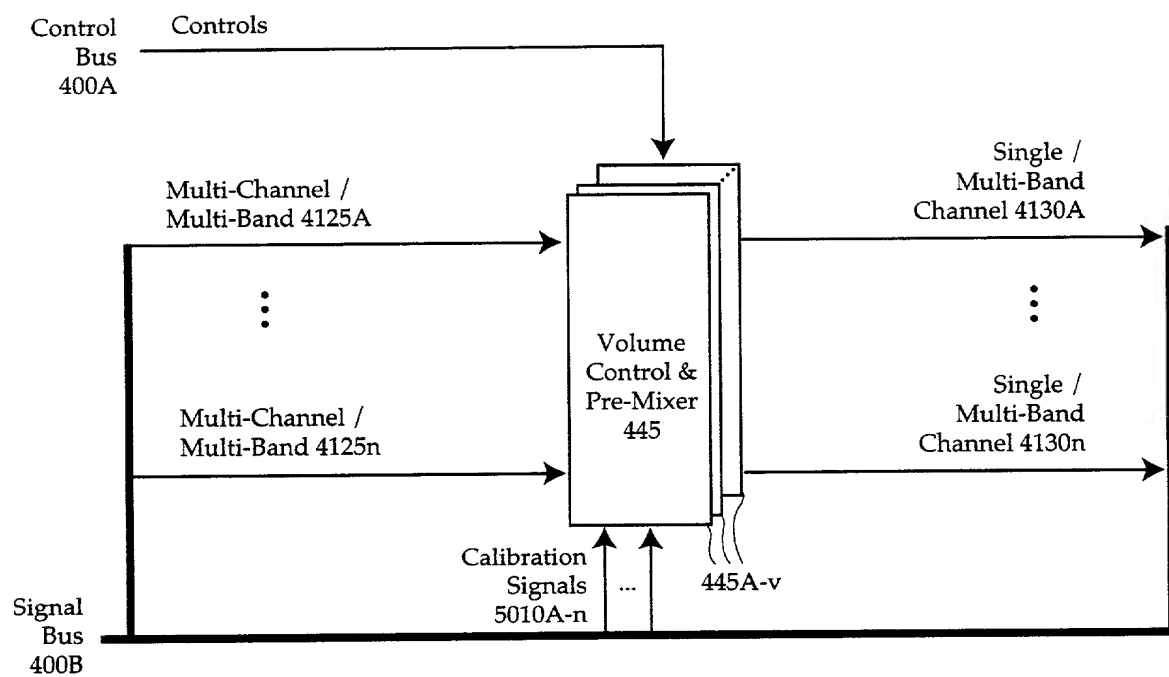


FIG. 41A

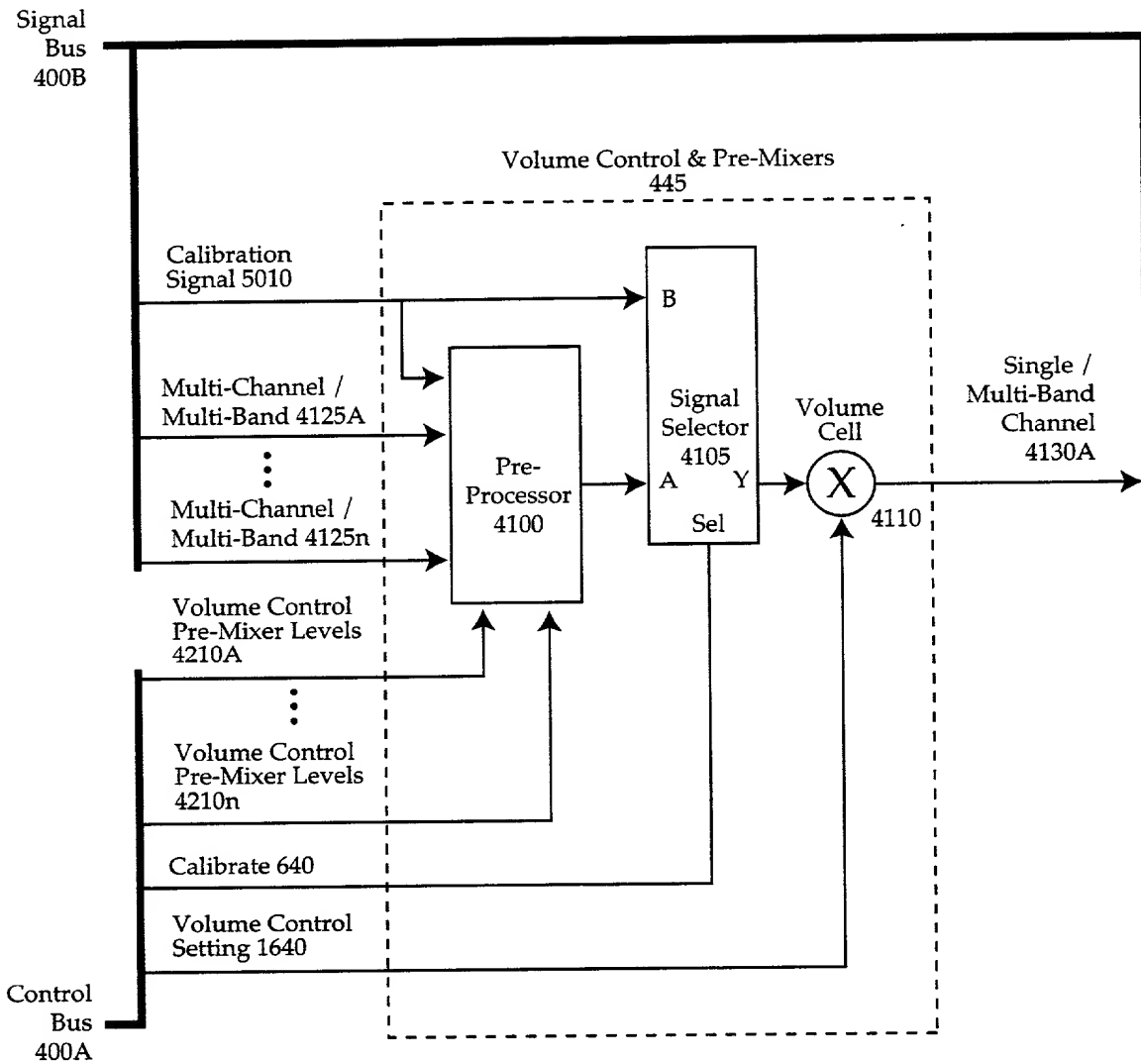


FIG. 41B

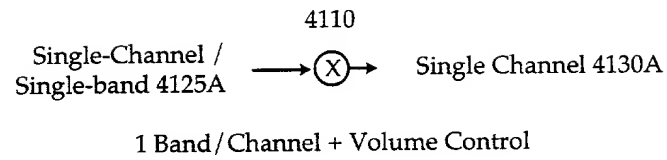


FIG. 42A

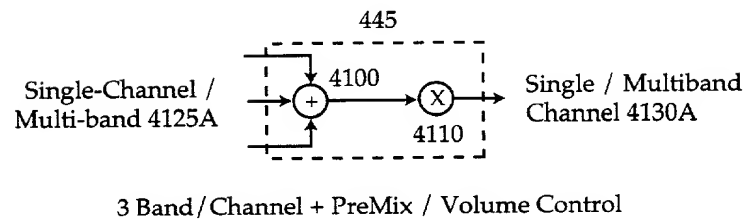
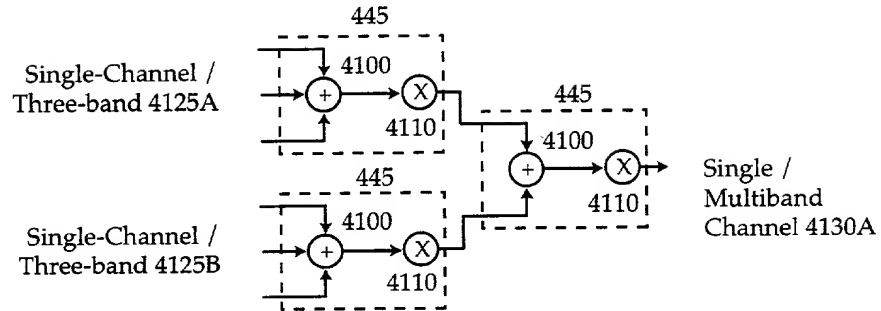
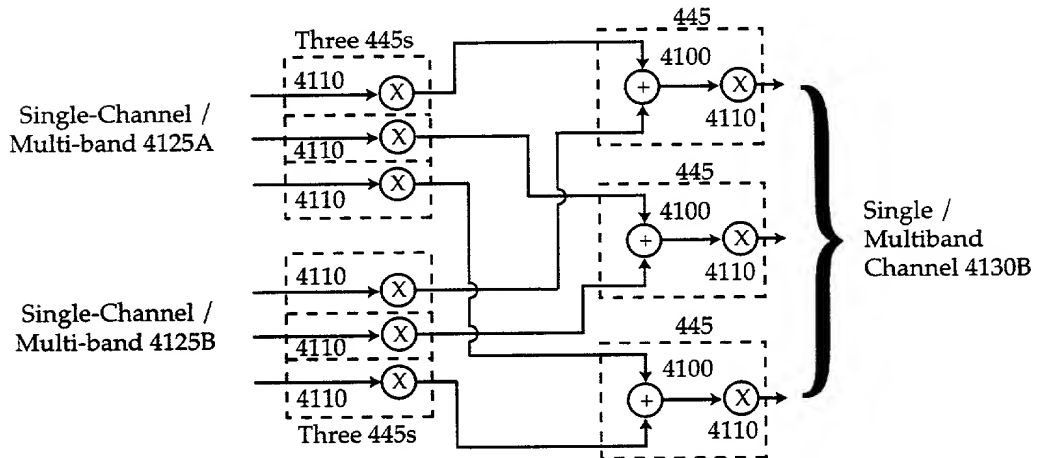


FIG. 42B



3 Band/Channel + Pre-Mix / Volume Control > Premix Volume Control
 3 Band/Channel + Pre-Mix / Volume Control > Premix Volume Control

FIG. 42C



3 Band/Channel + 3 Volume Control > 3 Premix Volume Control
 3 Band/Channel + 3 Volume Control > 3 Premix Volume Control

FIG. 42D

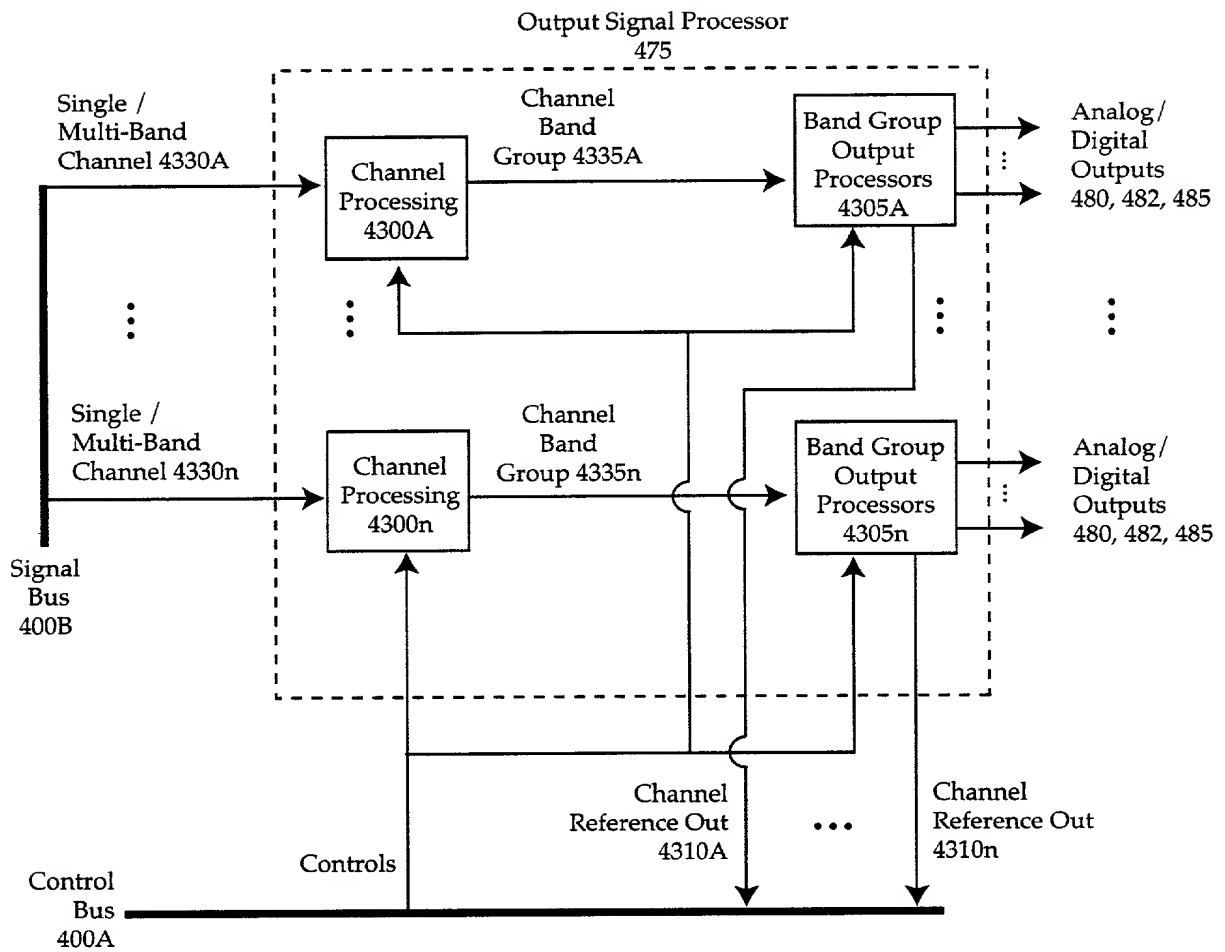


FIG. 43A

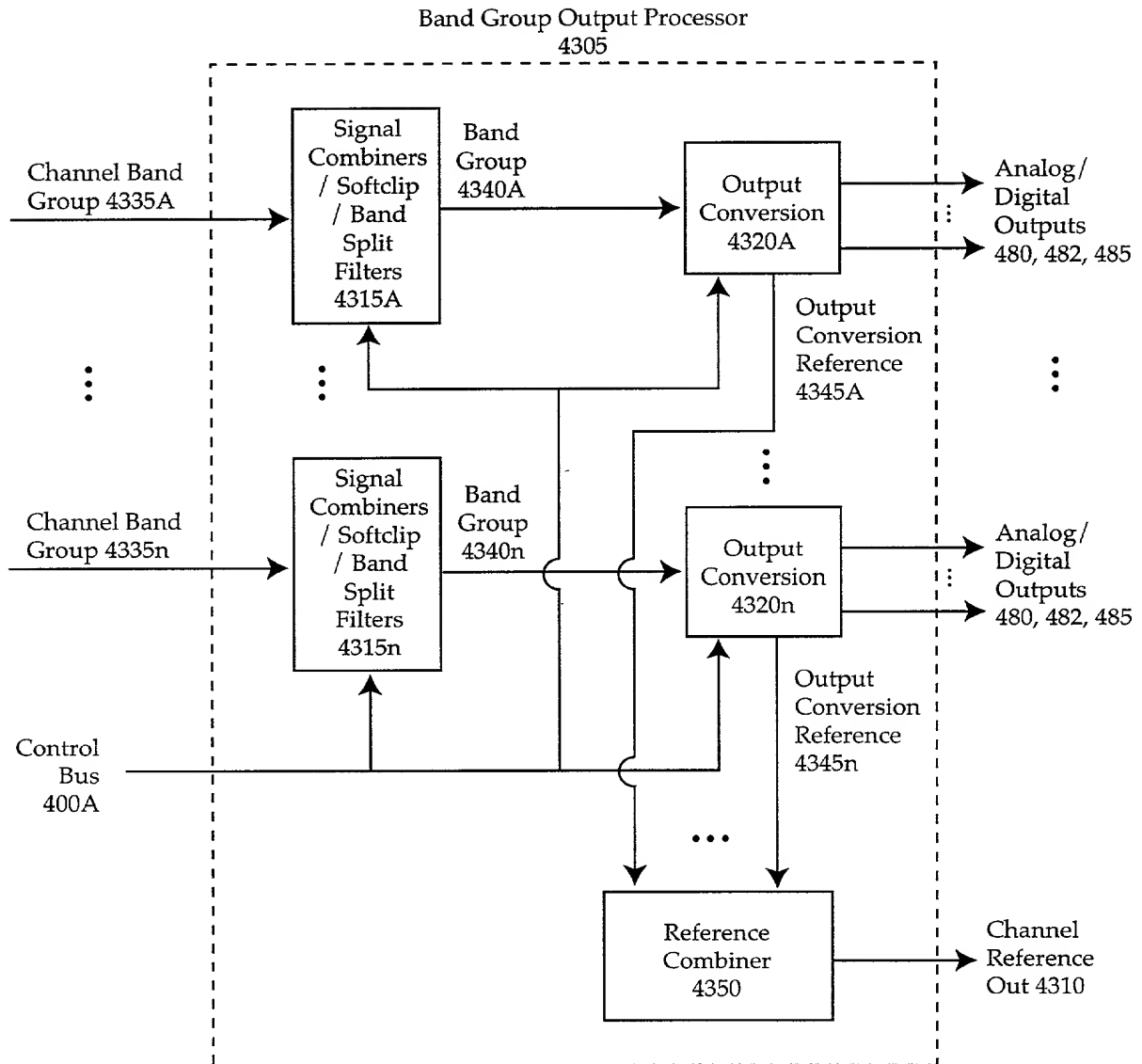


FIG. 43B

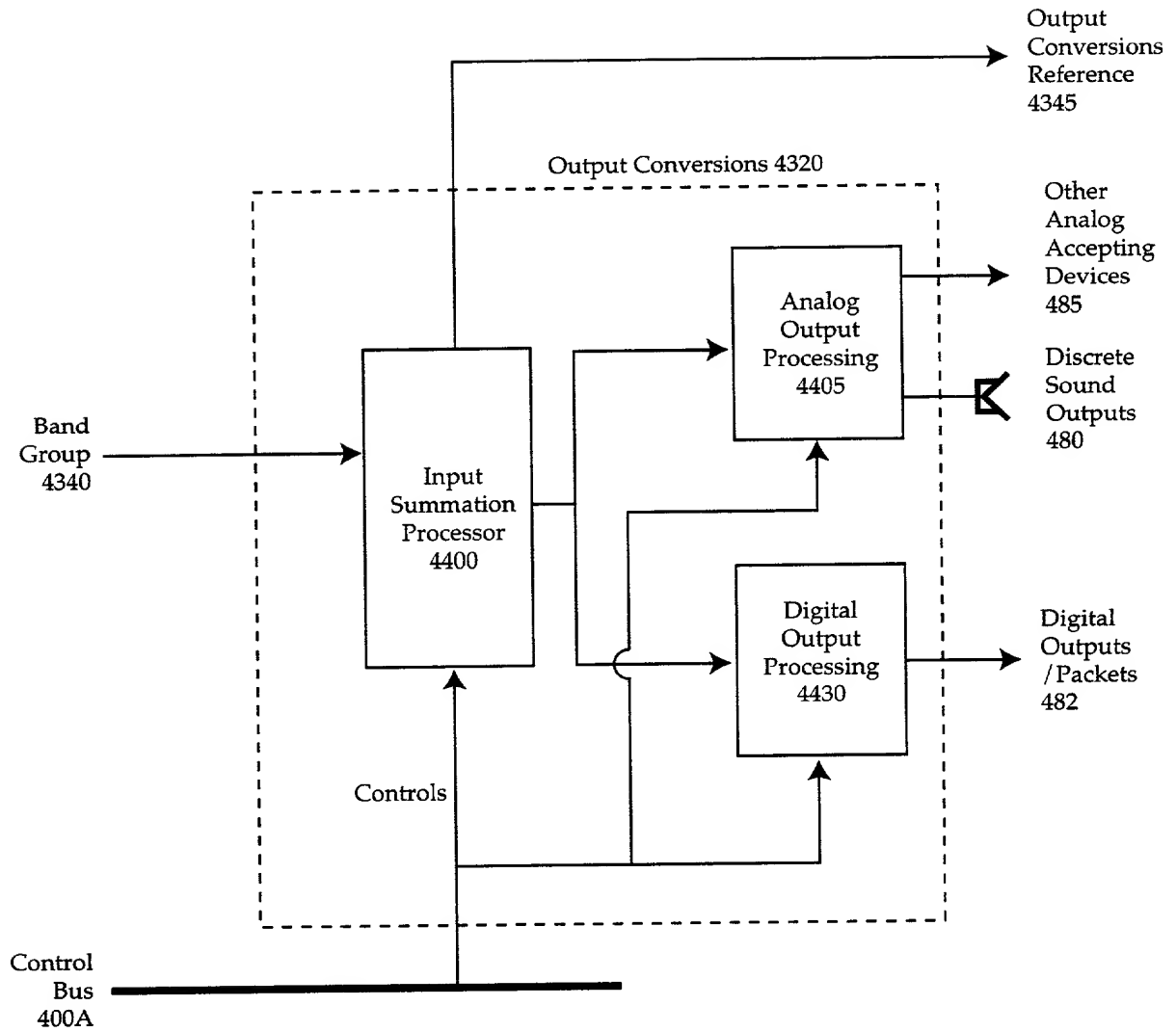


FIG. 44

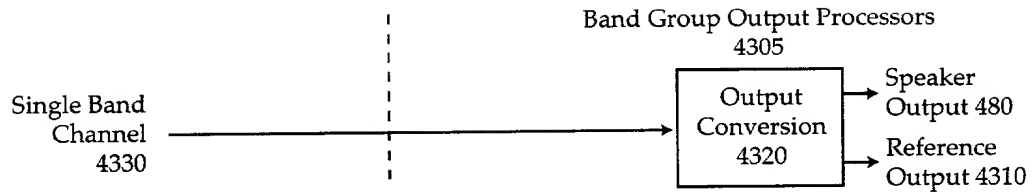


FIG. 45A

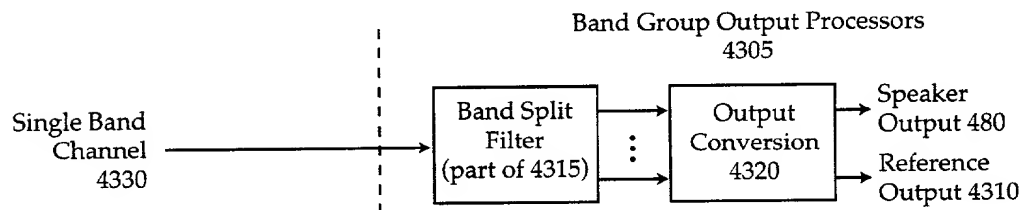


FIG. 45B

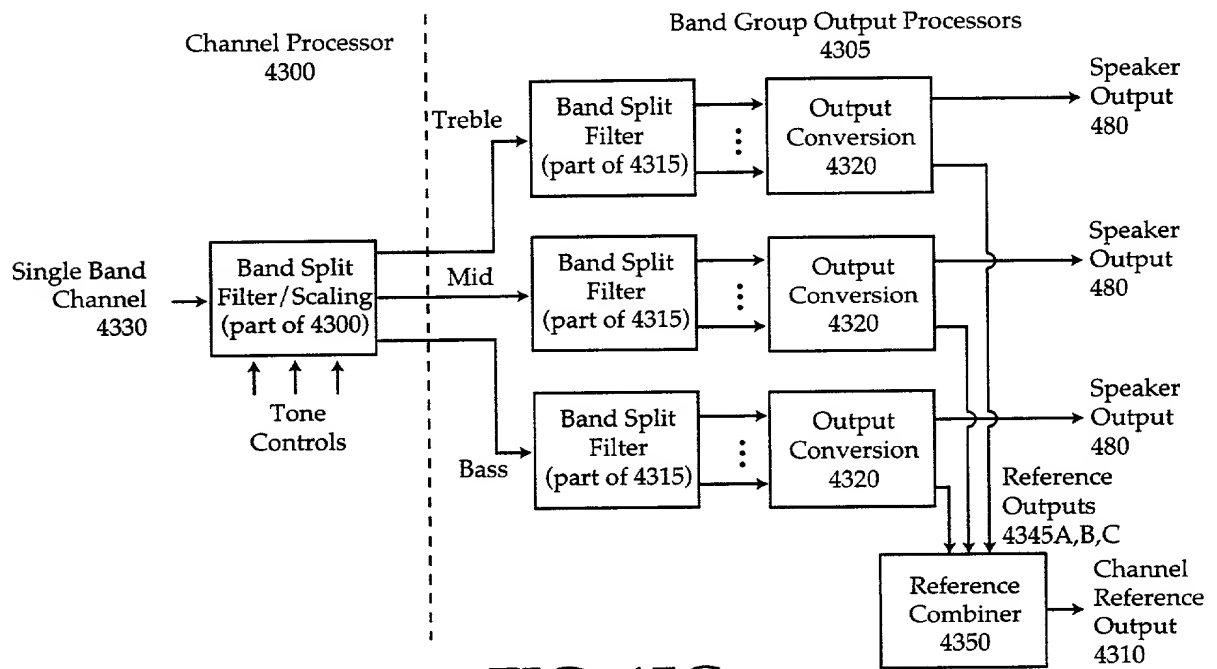


FIG. 45C

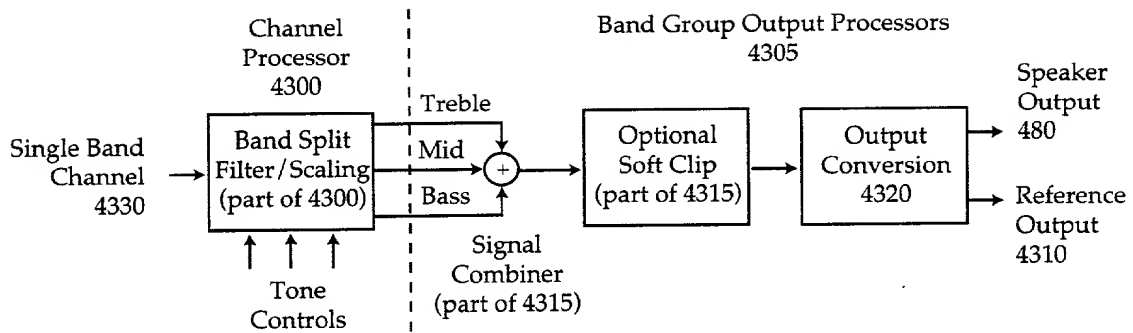


FIG. 45D

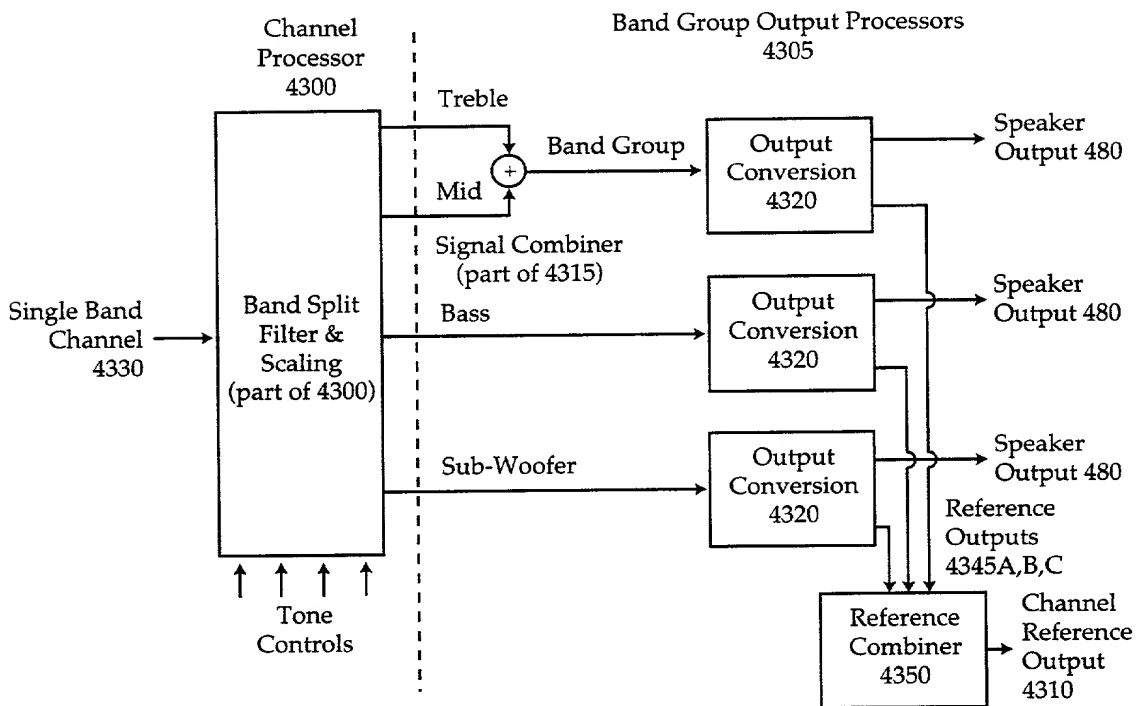


FIG. 45E

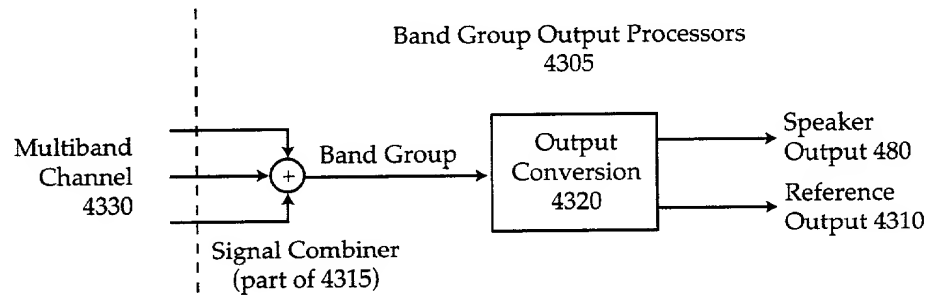


FIG. 45F

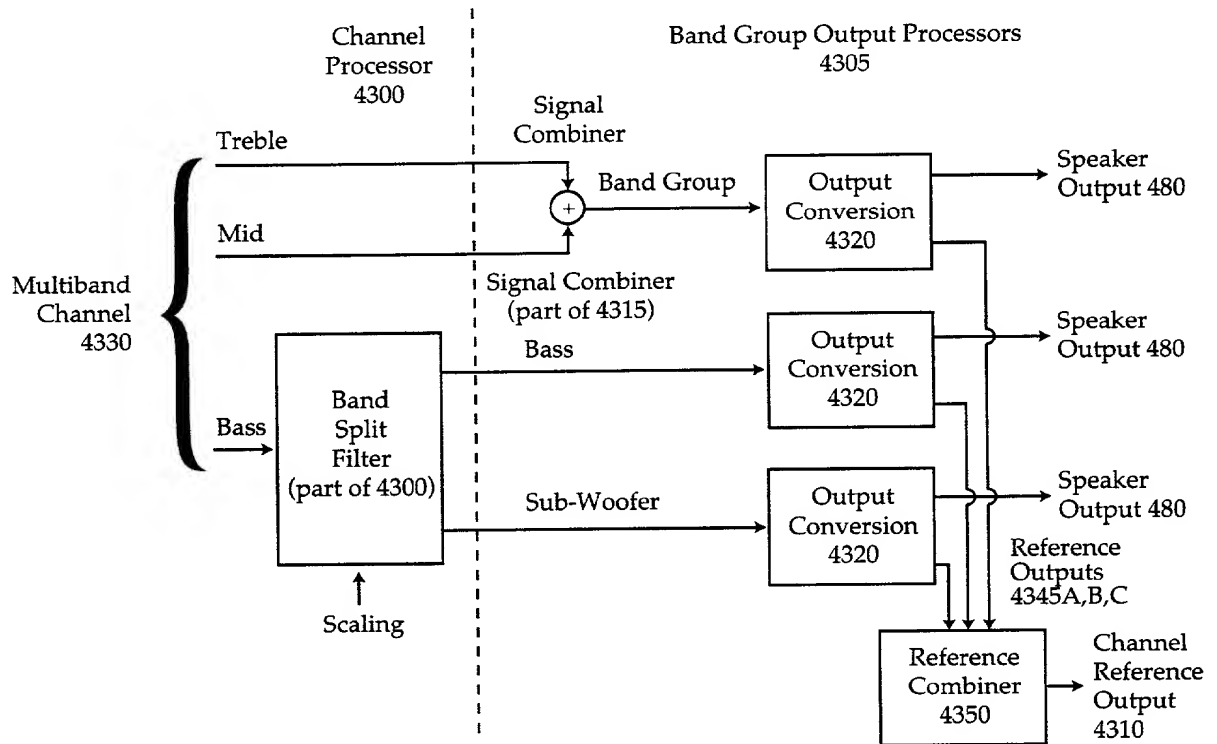


FIG. 45G

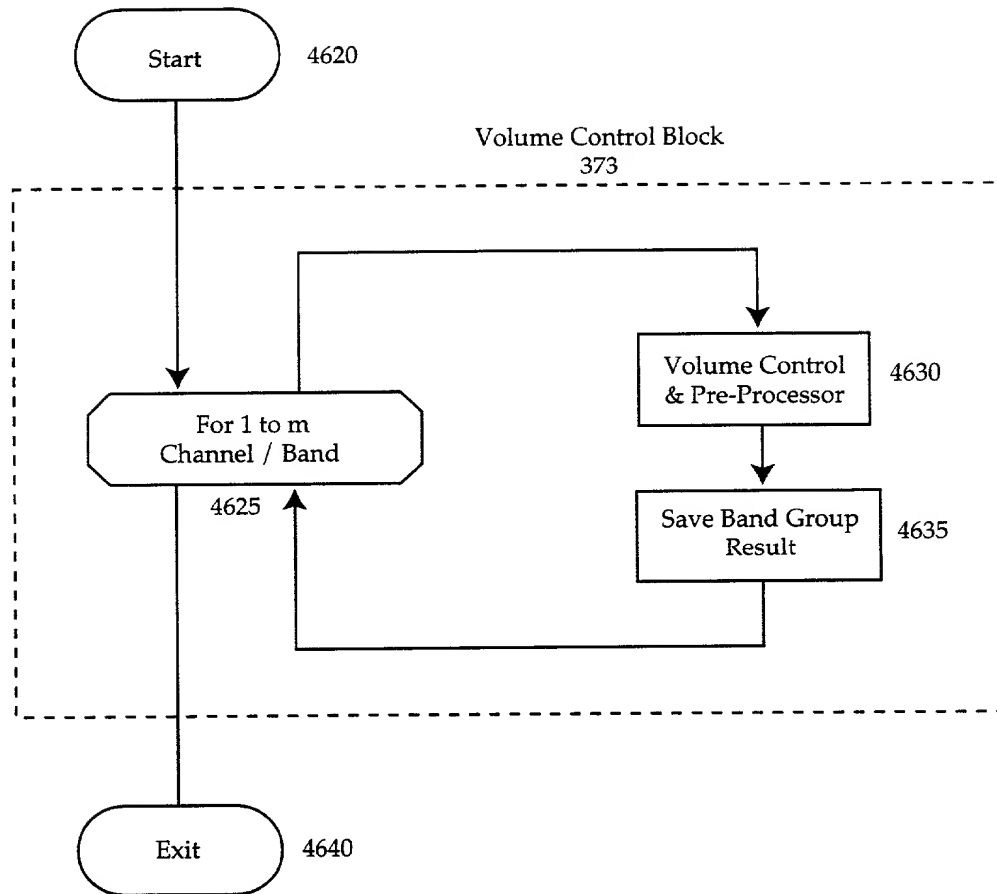


FIG. 46

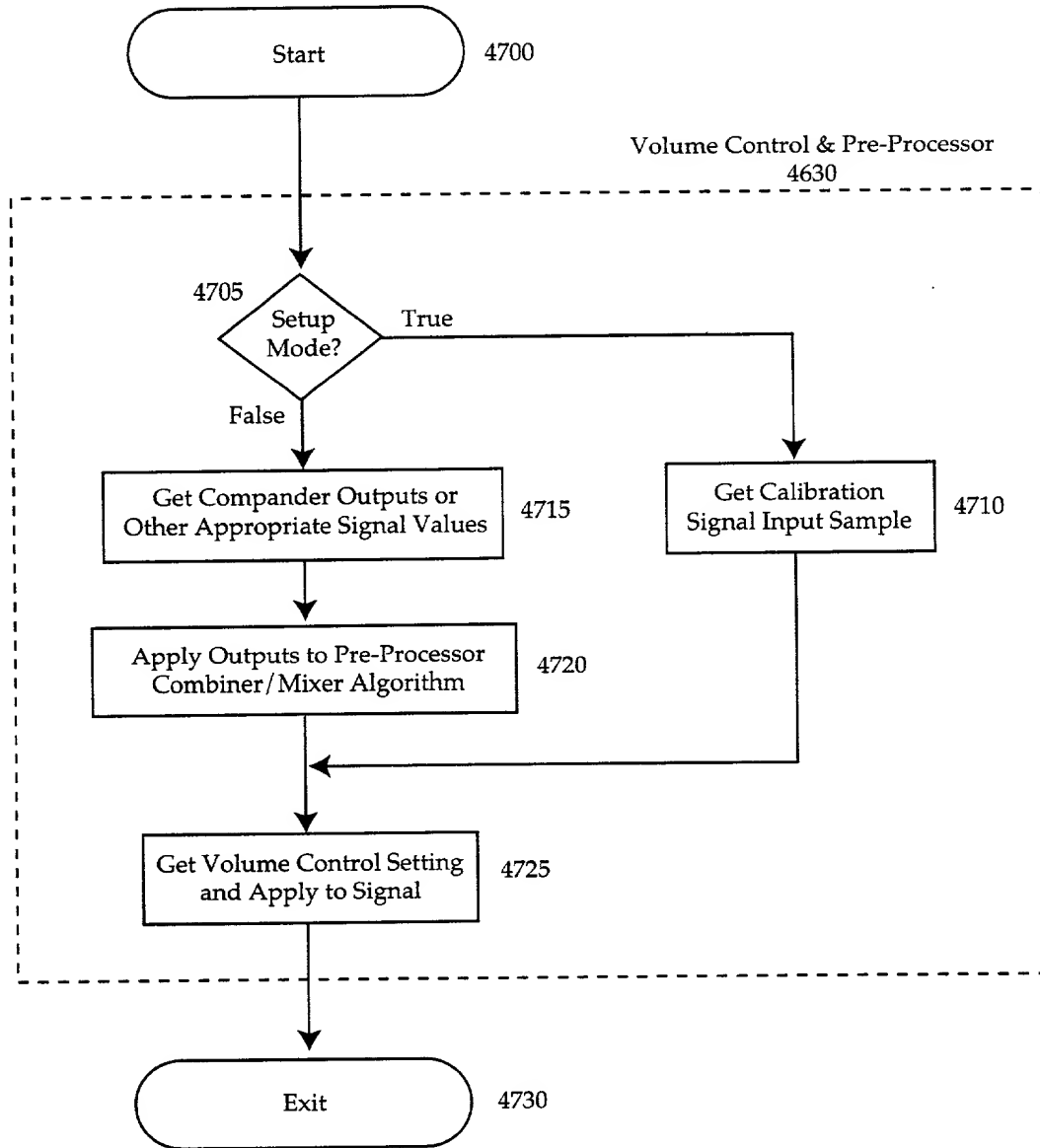


FIG. 47

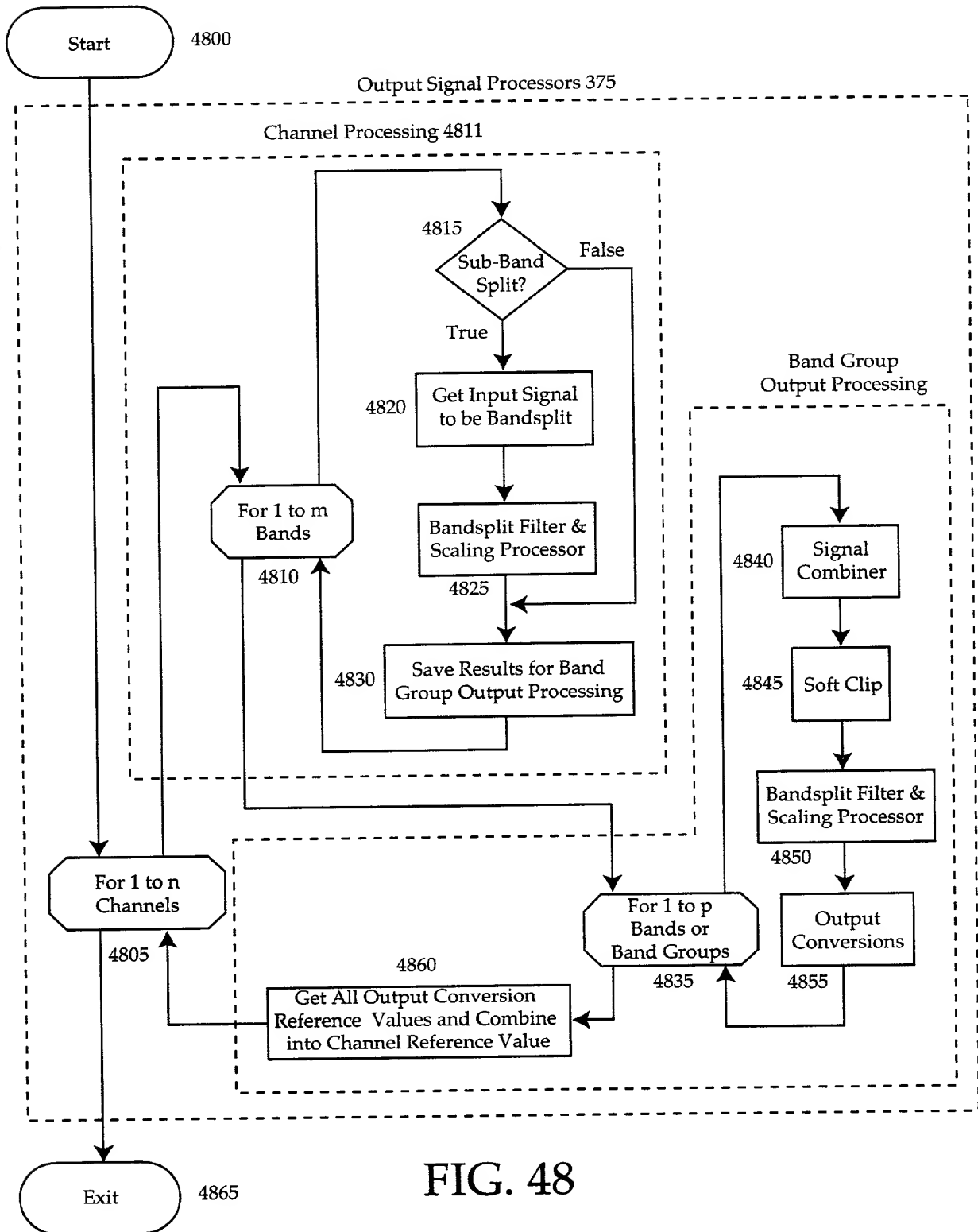


FIG. 48

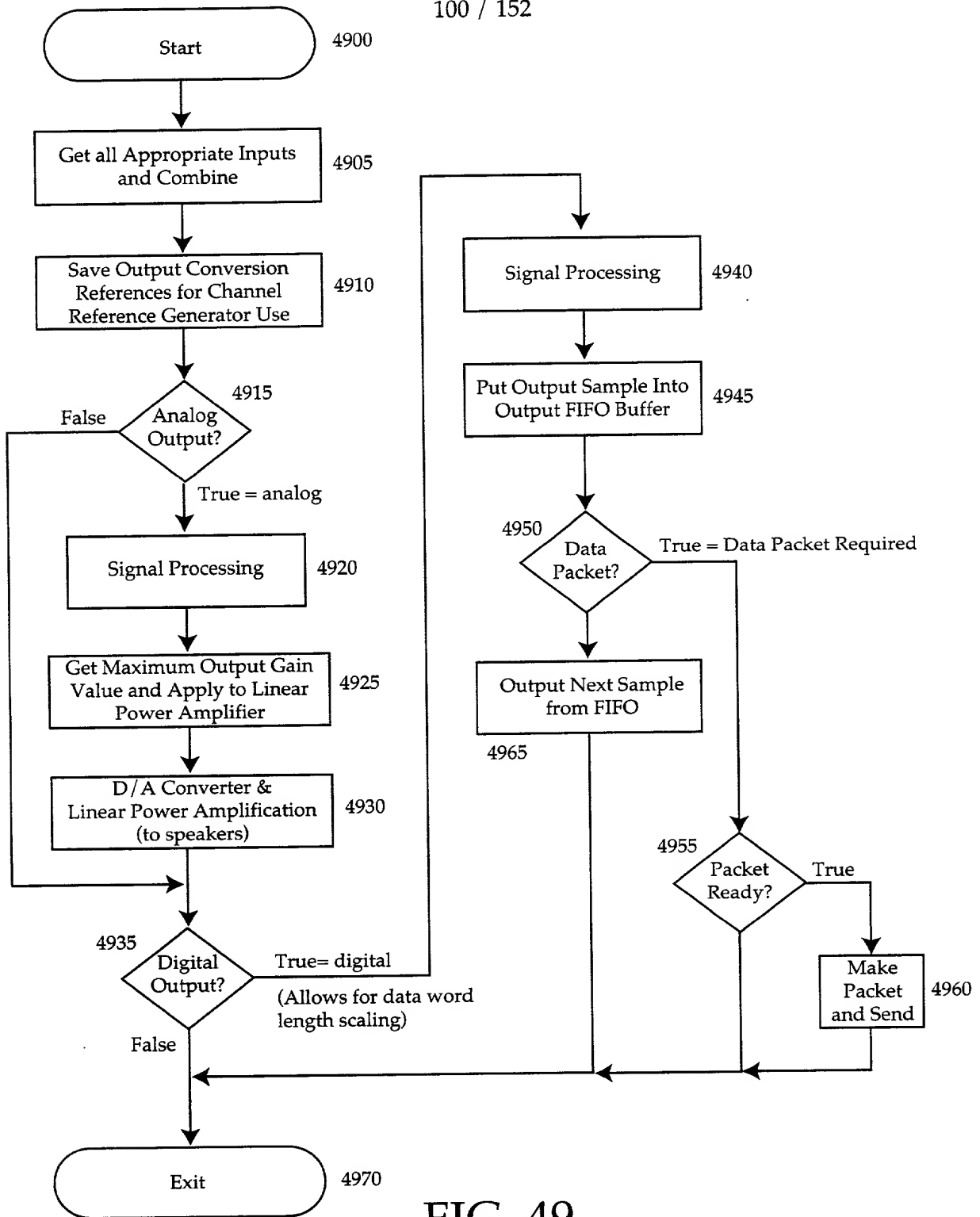


FIG. 49

Calibrator / Annunciator 420

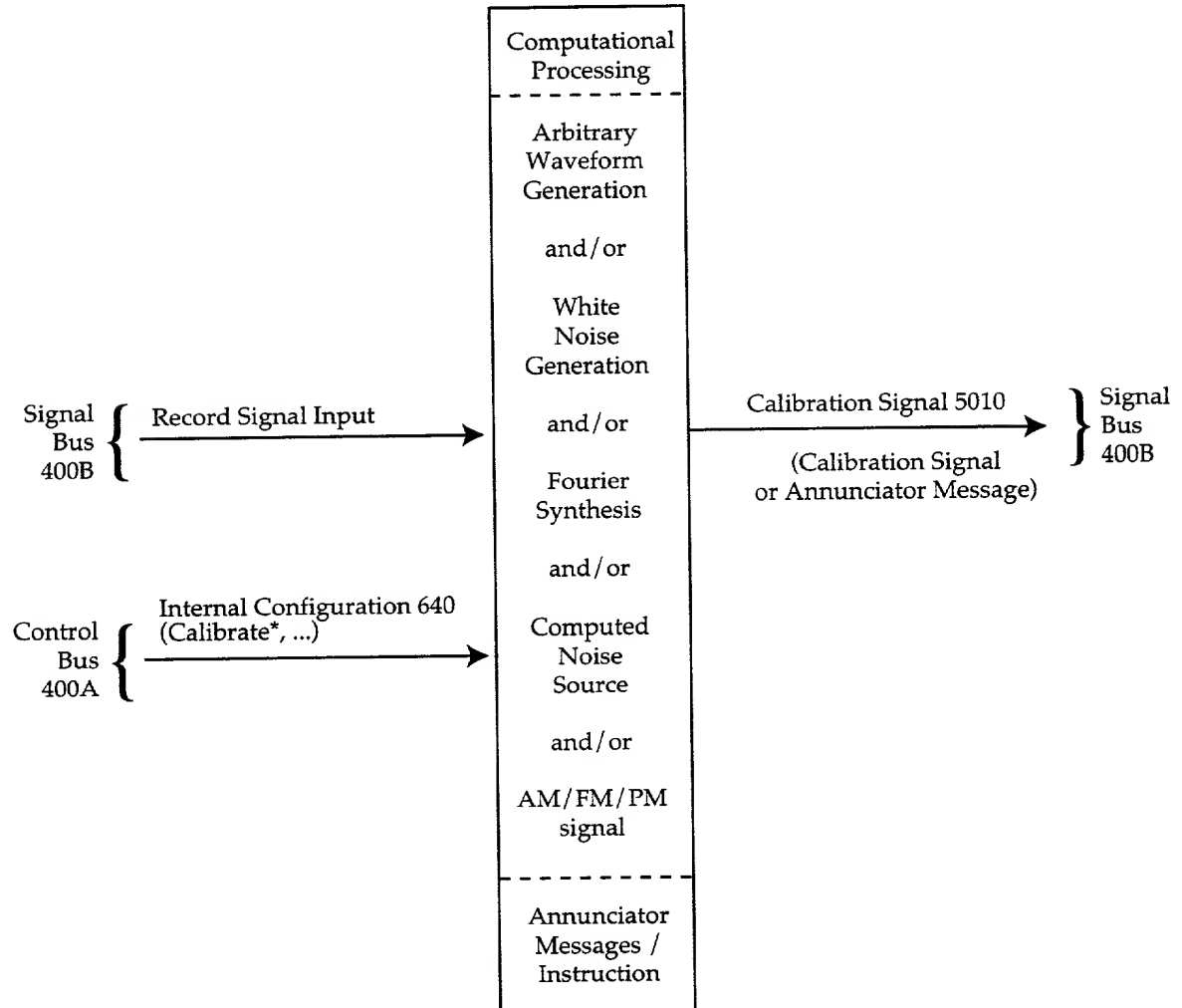


FIG. 50

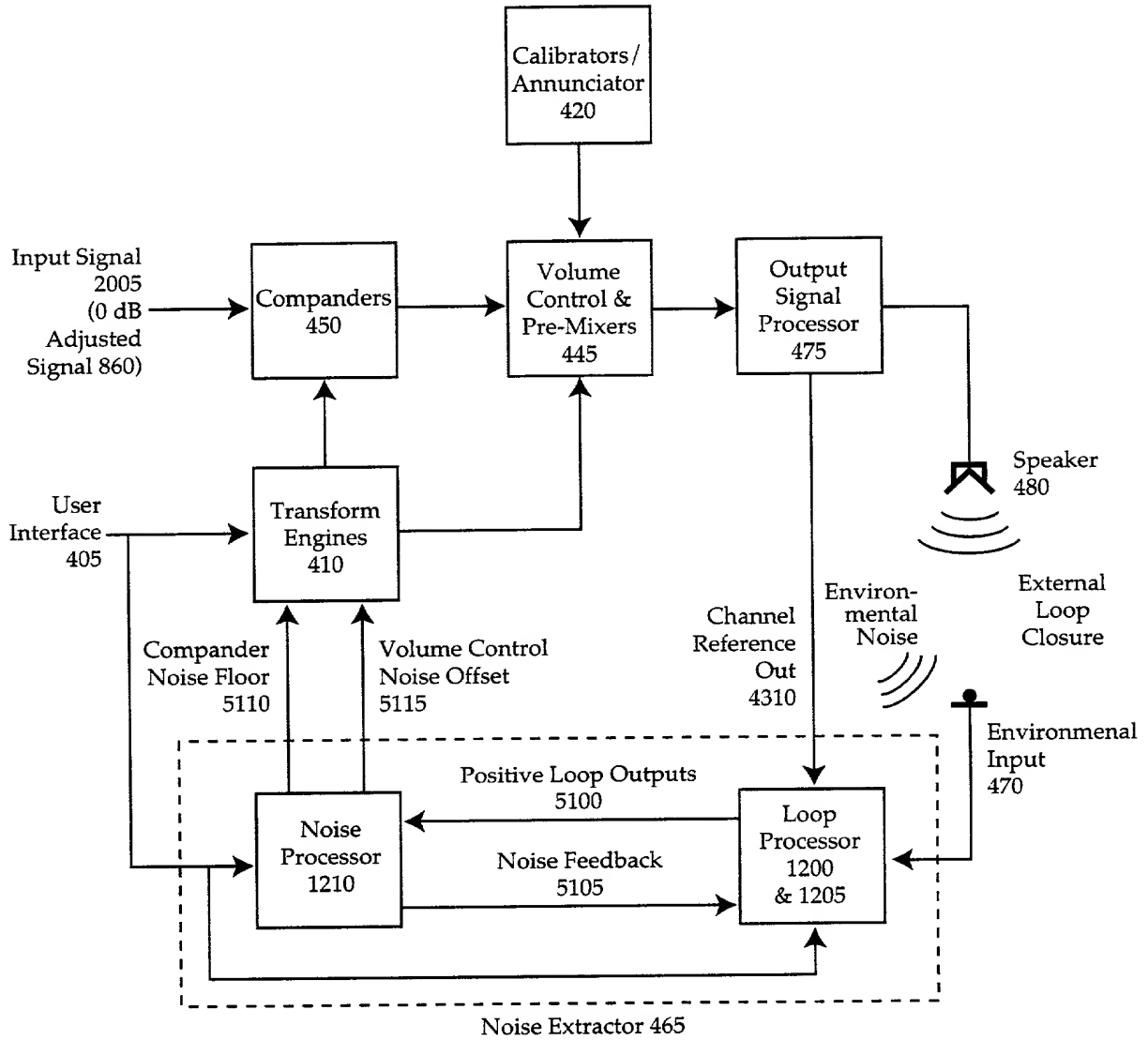


FIG. 51

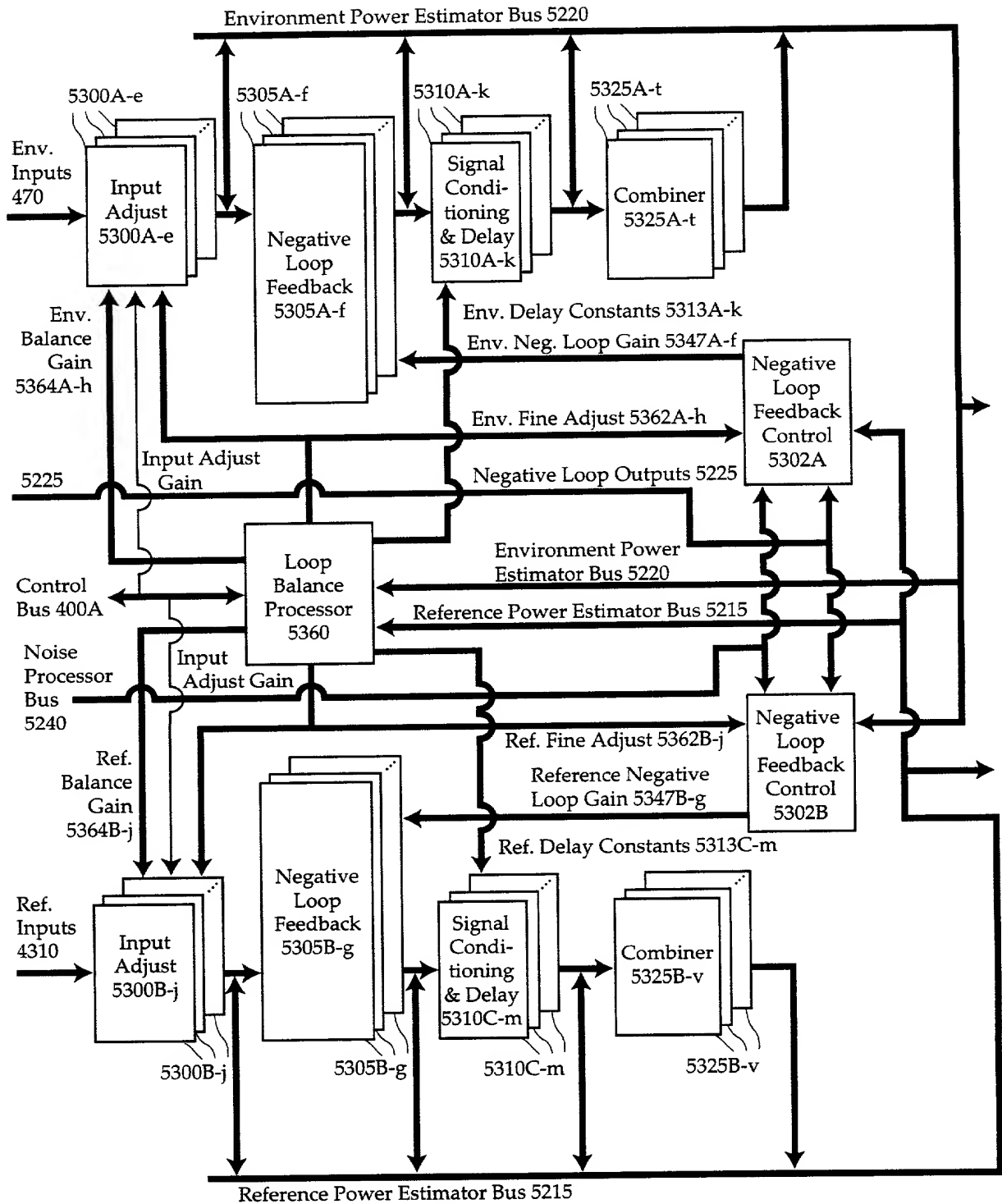


FIG. 52A

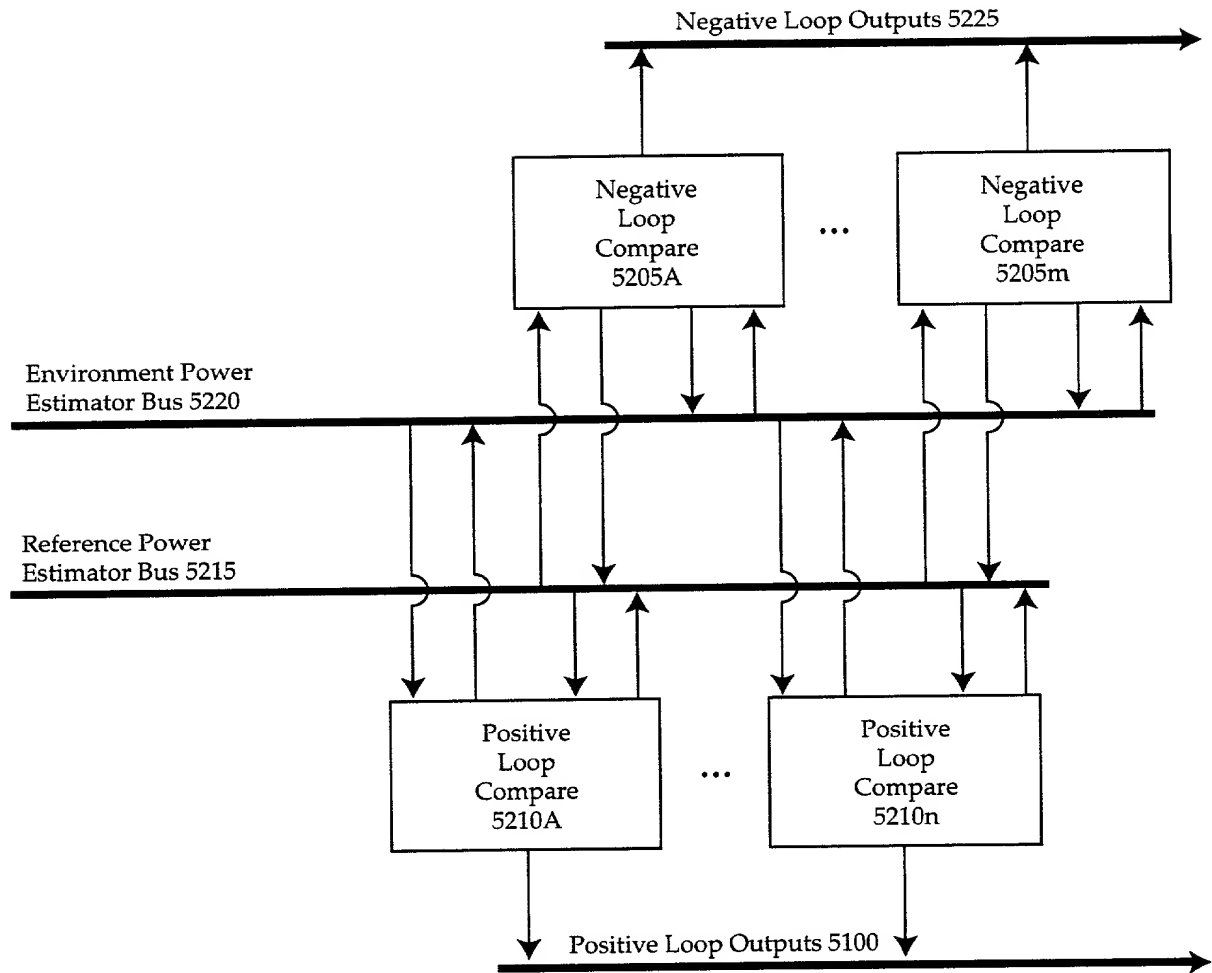


FIG. 52B

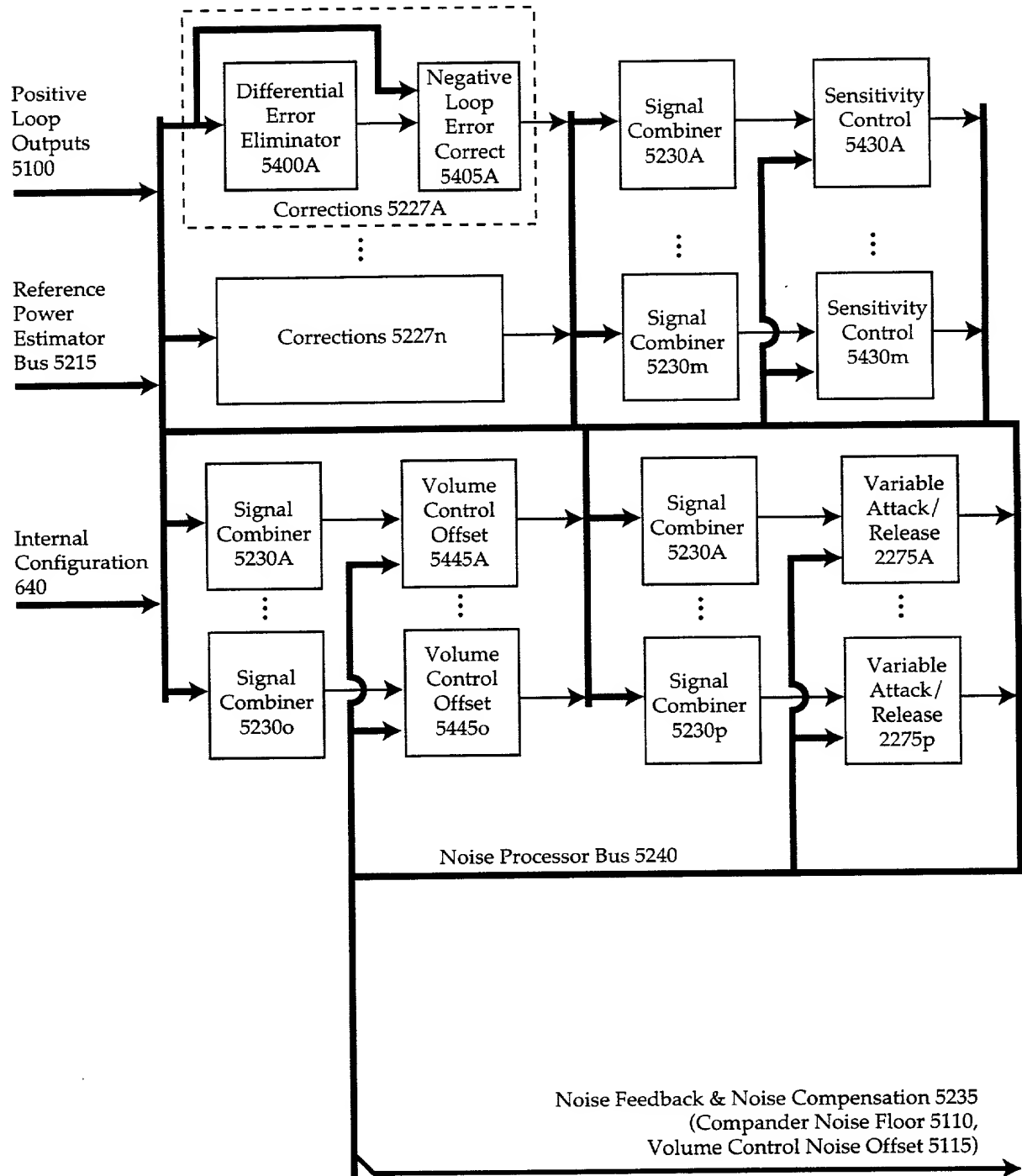


FIG. 52C



L

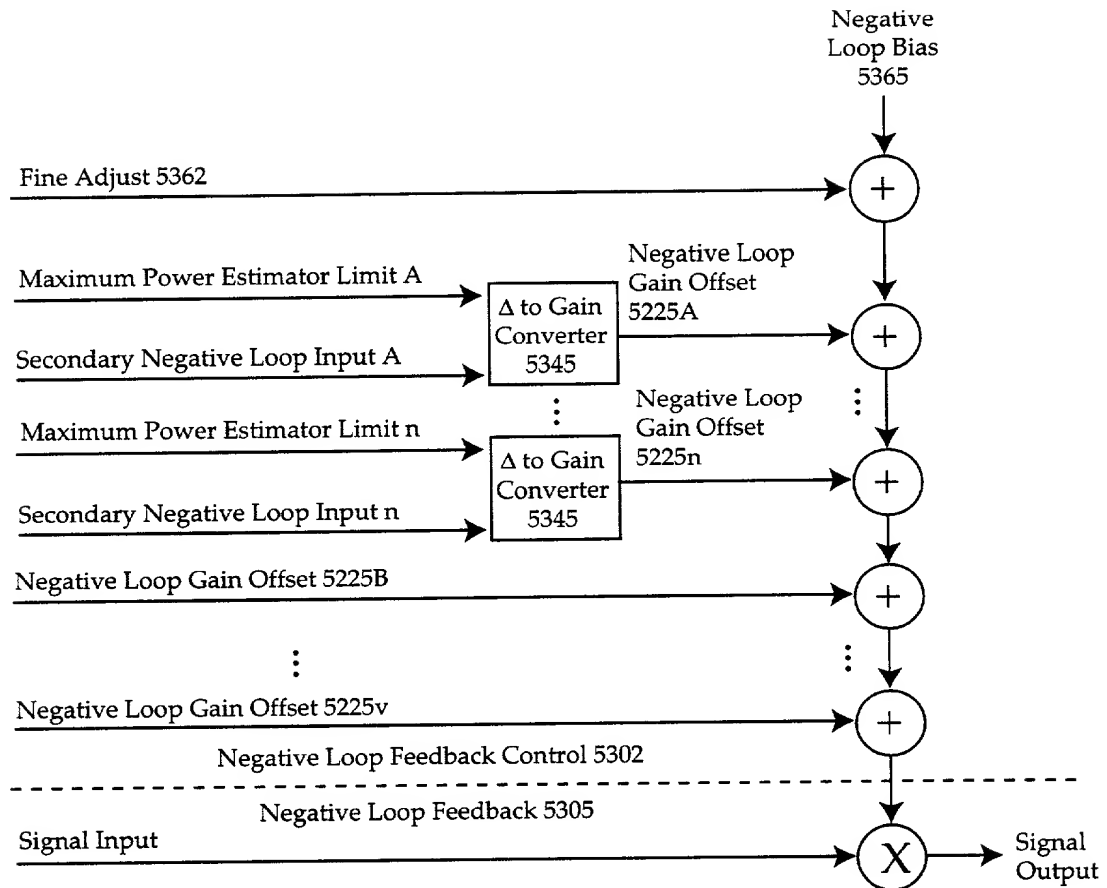


FIG. 53B

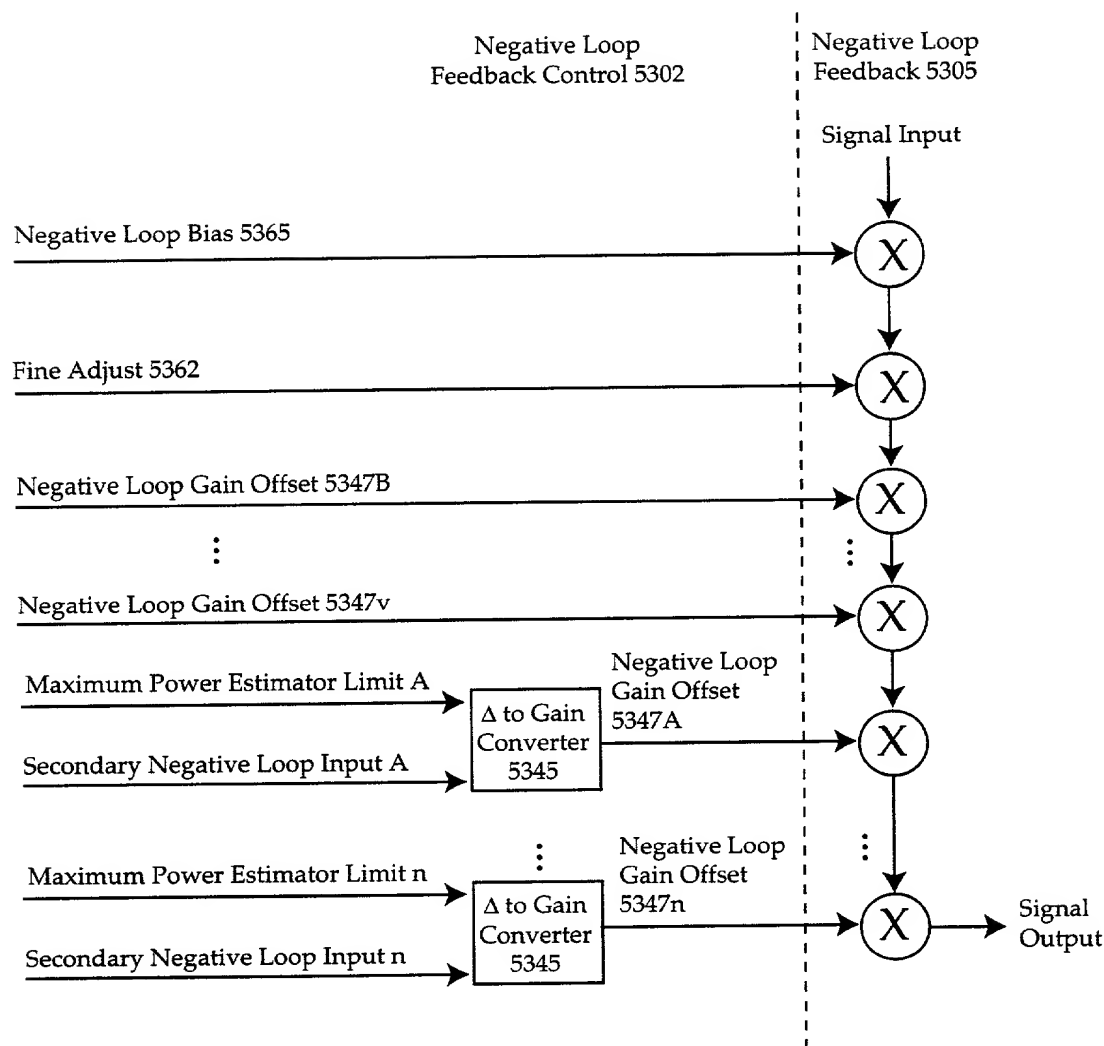


FIG. 53C

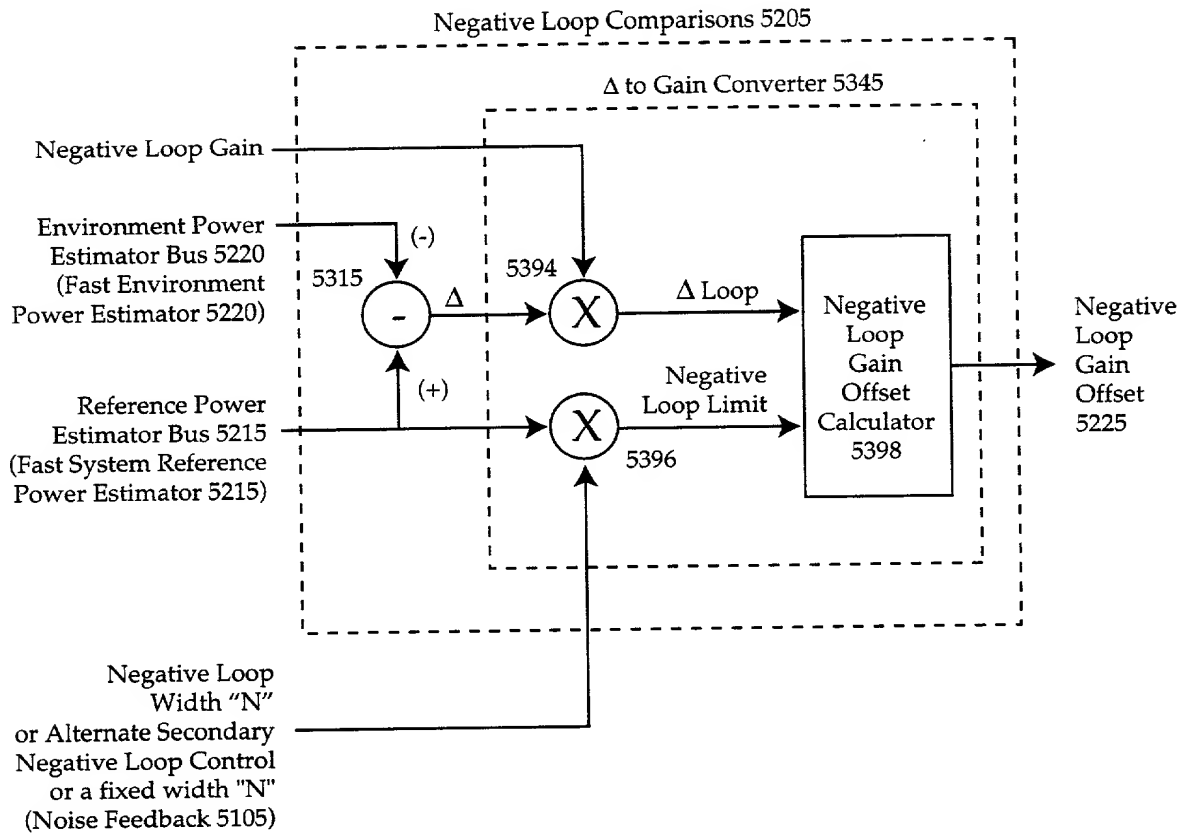


FIG. 53D

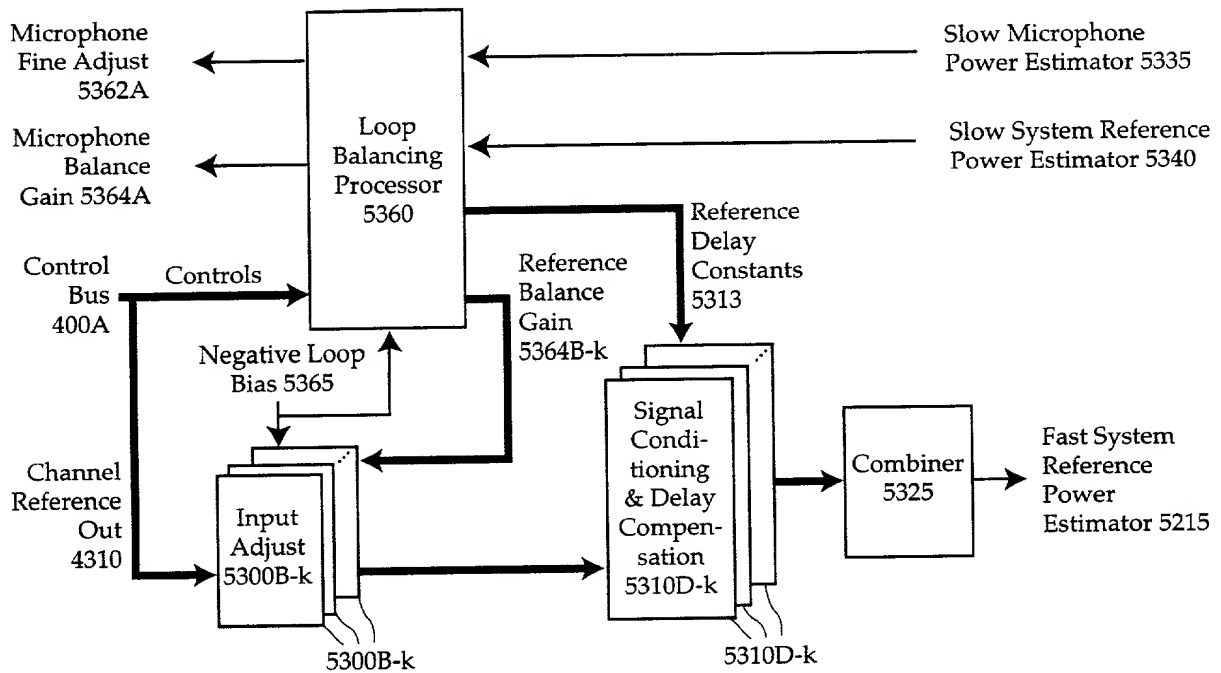


FIG. 53E

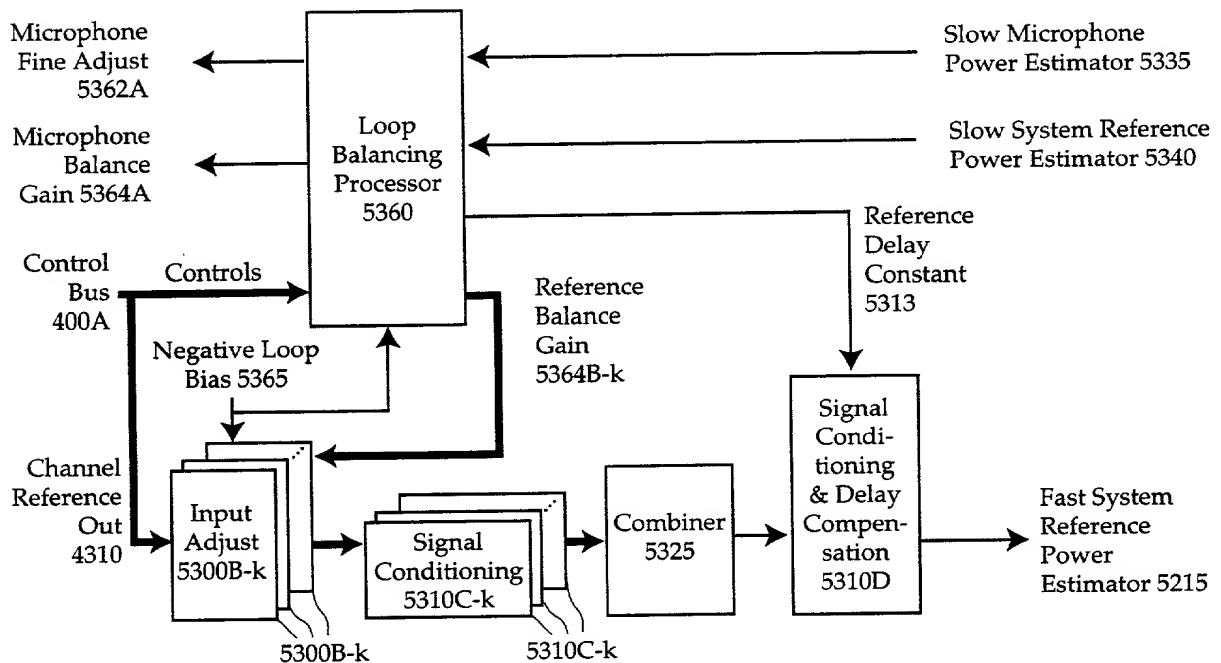


FIG. 53F

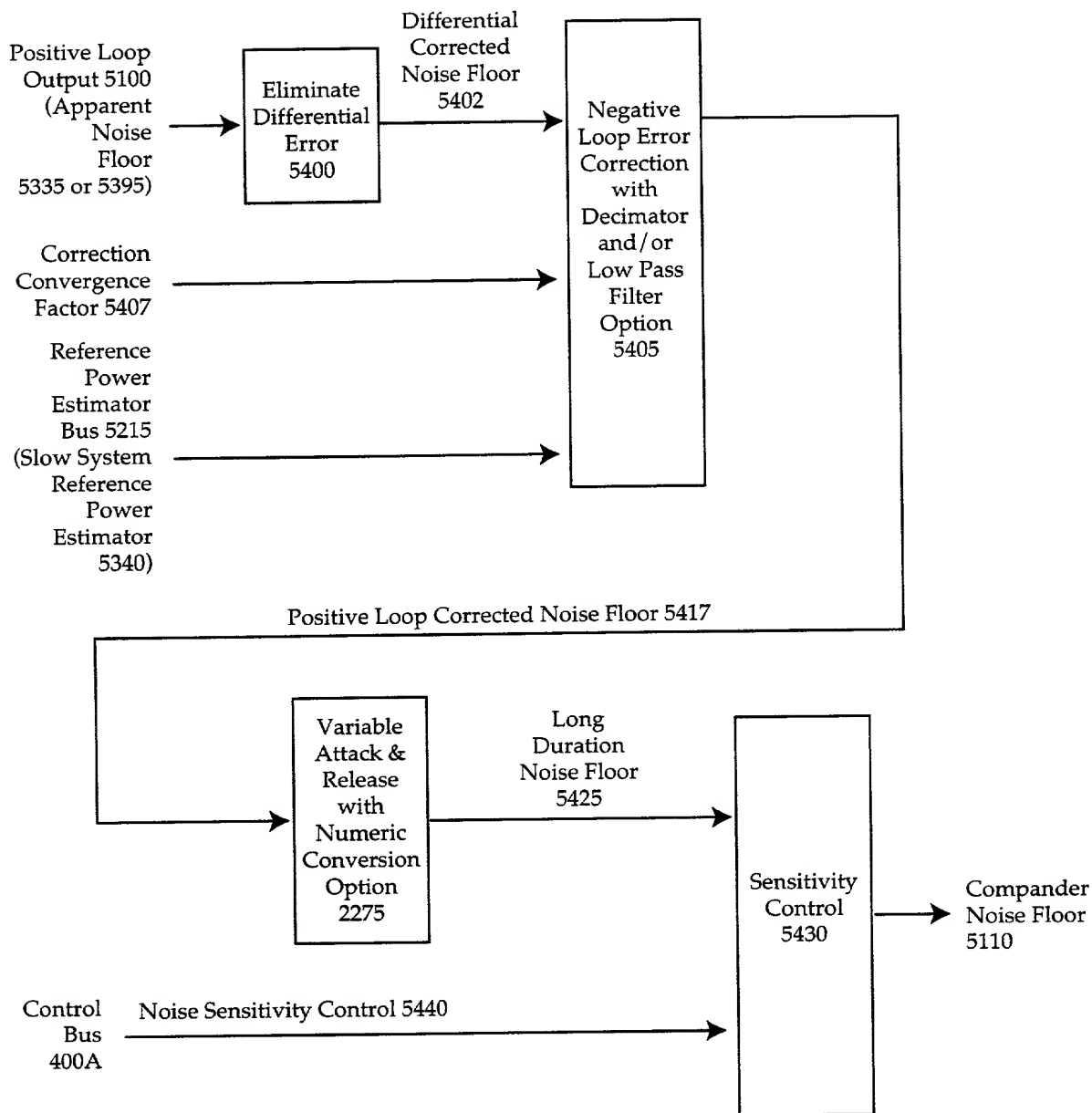


FIG. 54A

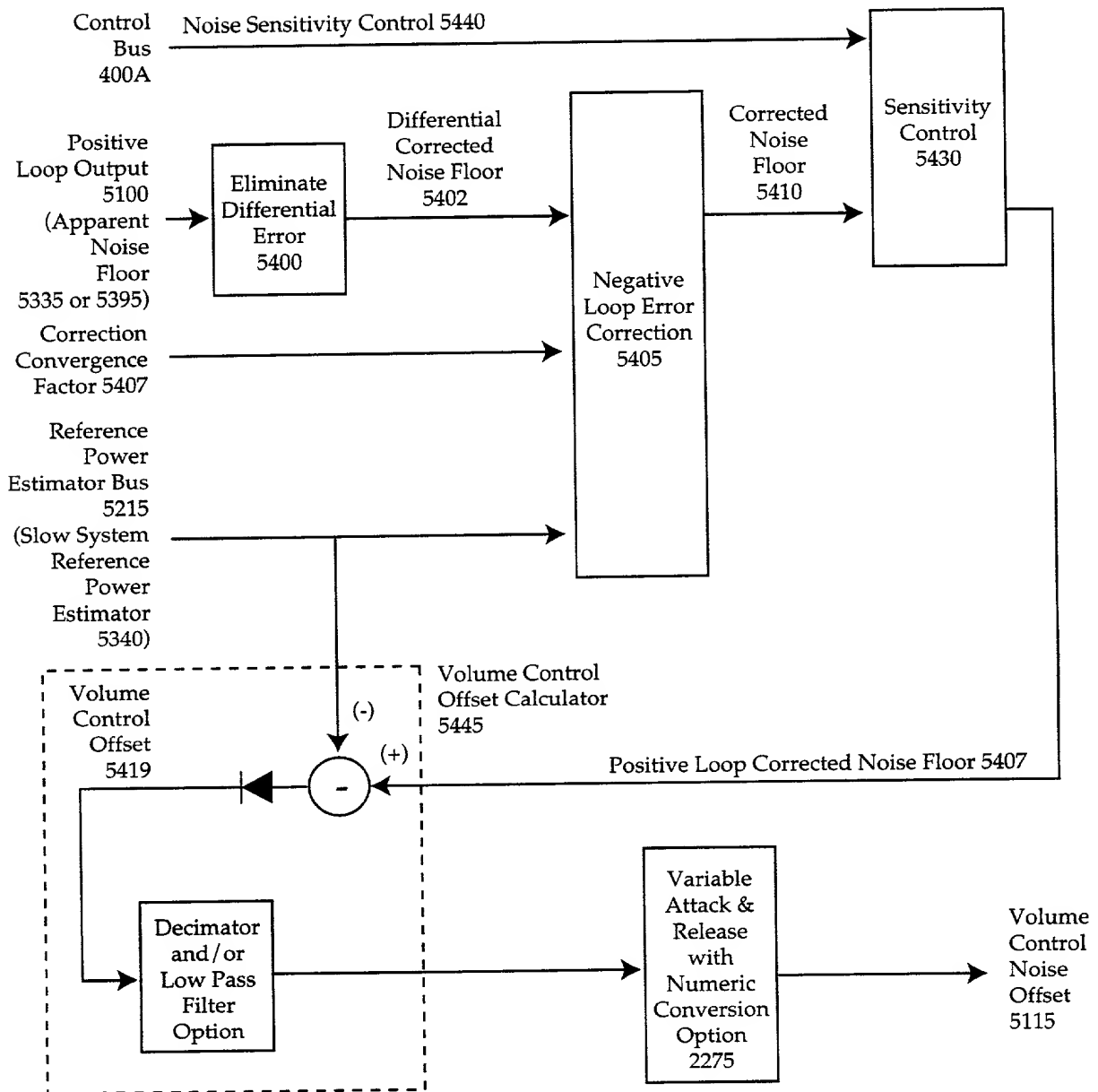


FIG. 54B

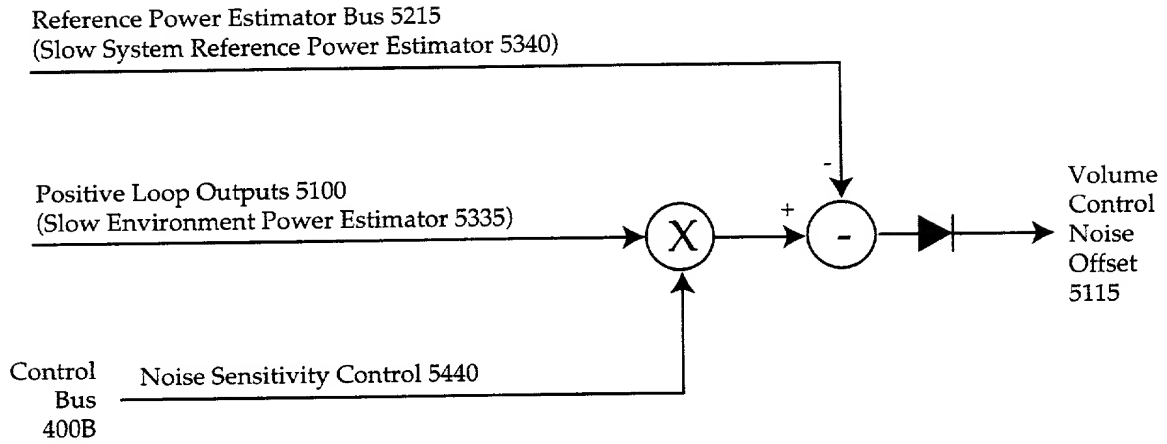


FIG. 54C

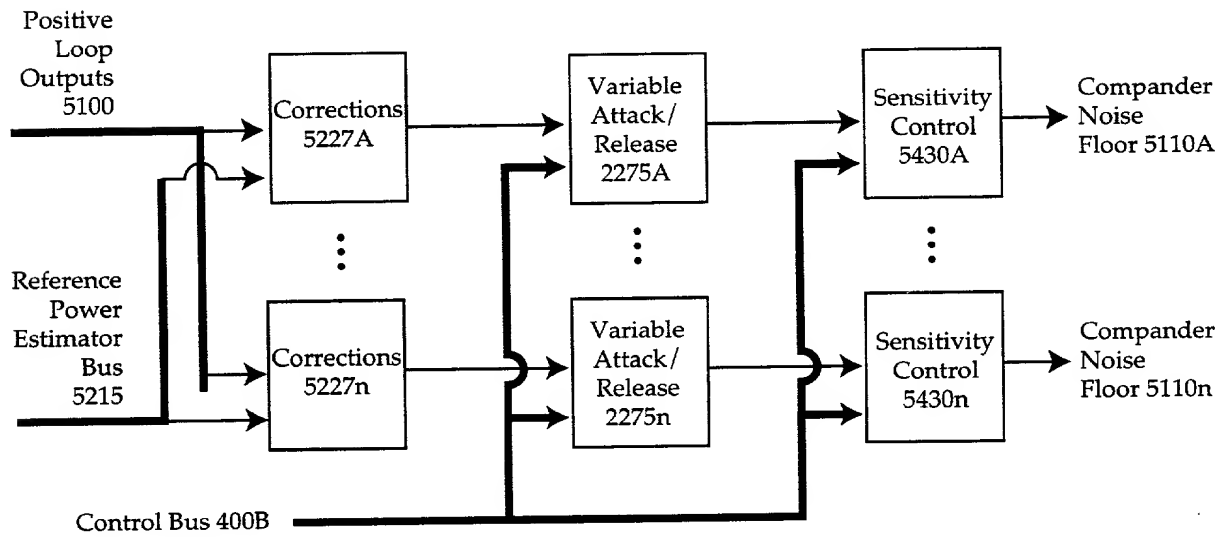


FIG. 54D

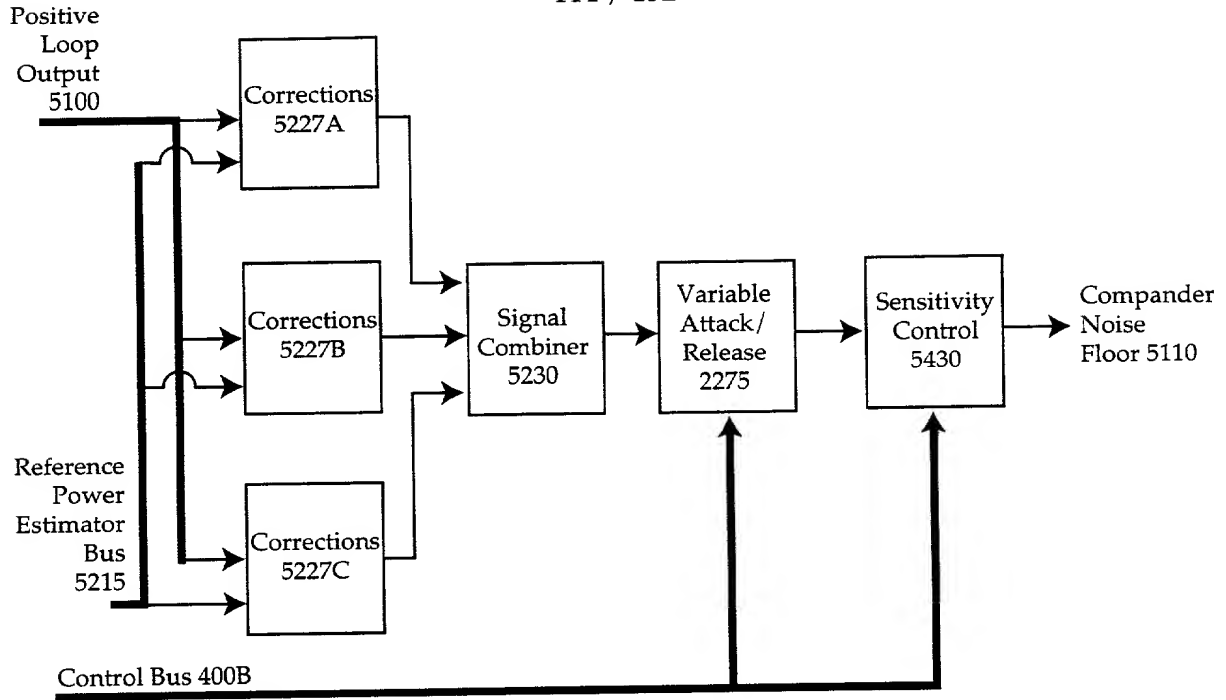


FIG. 54E

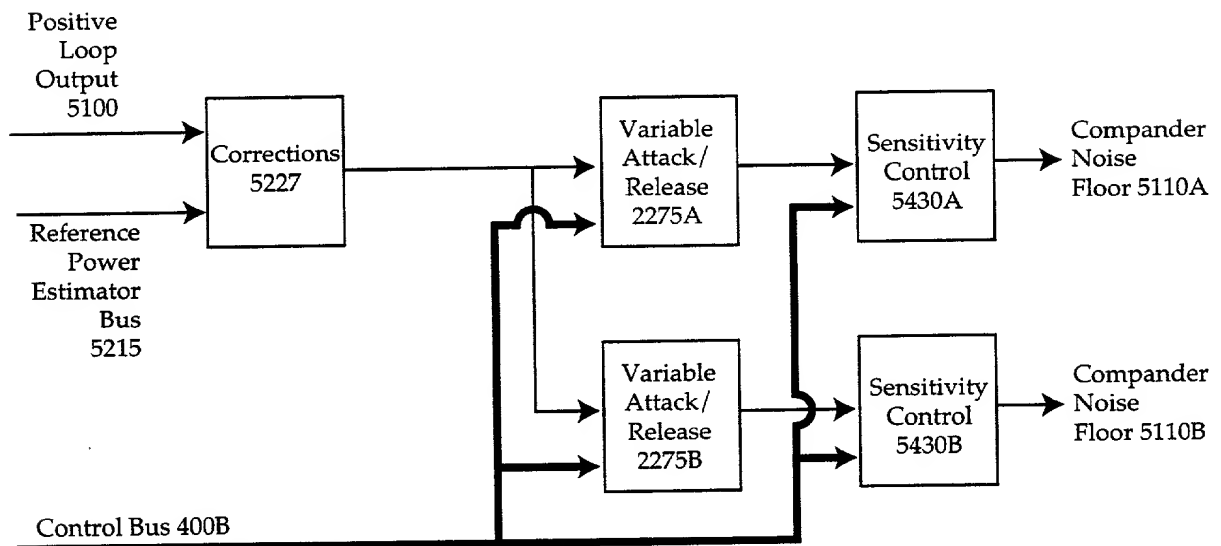


FIG. 54F

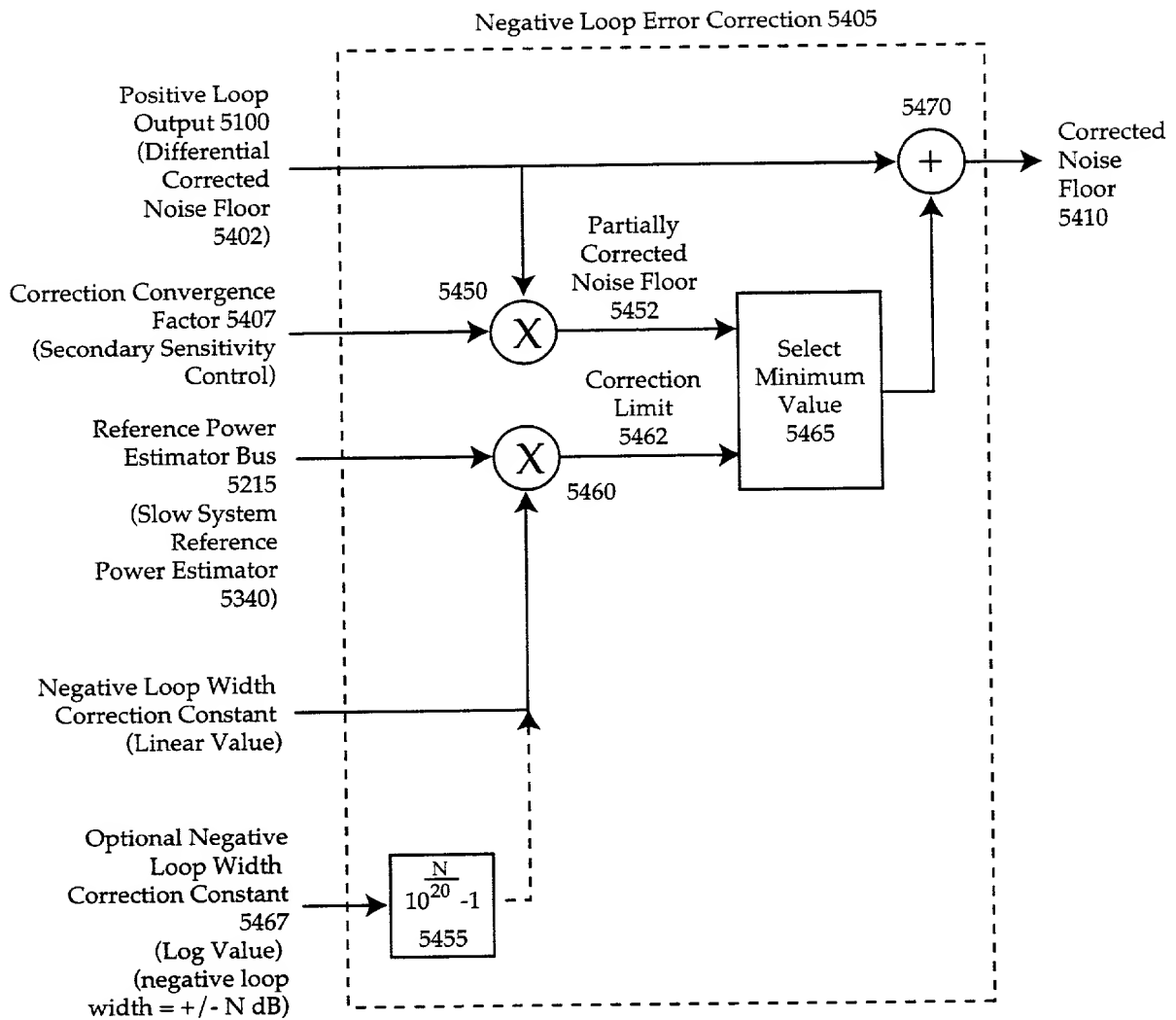


FIG. 54G

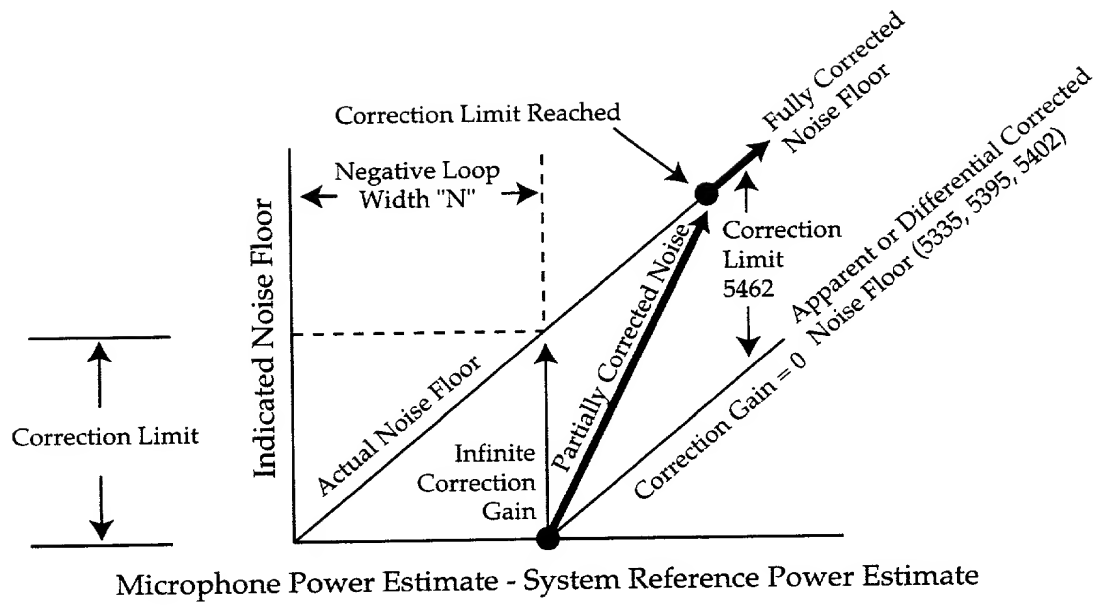


FIG. 54H

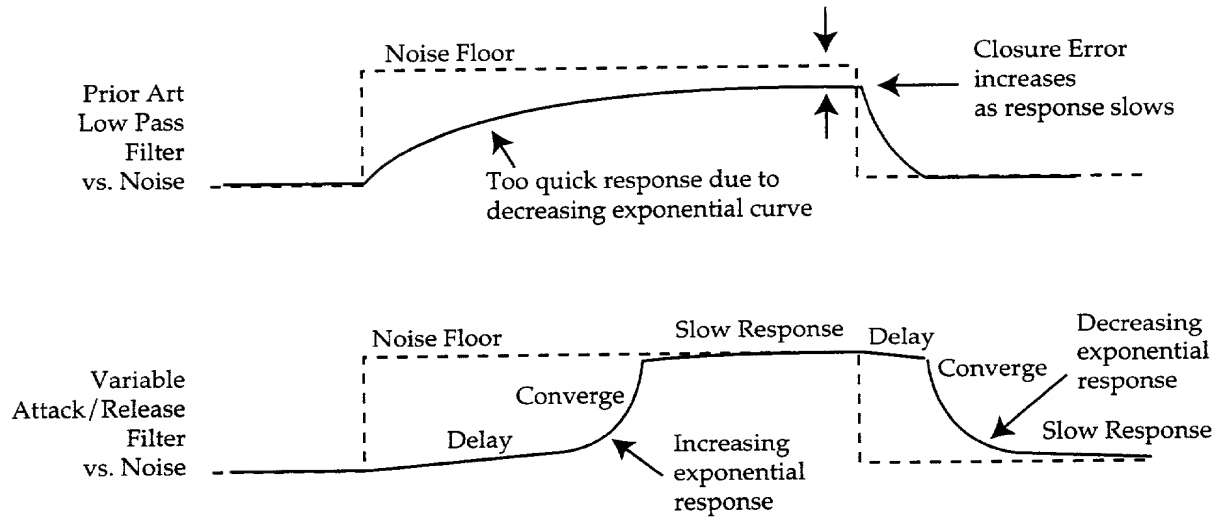


FIG. 55A

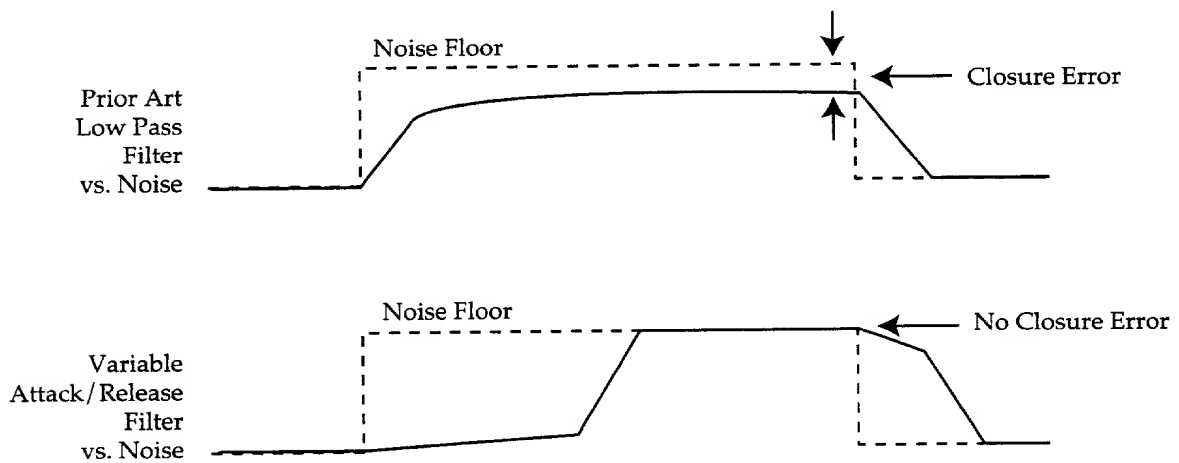


FIG. 55B

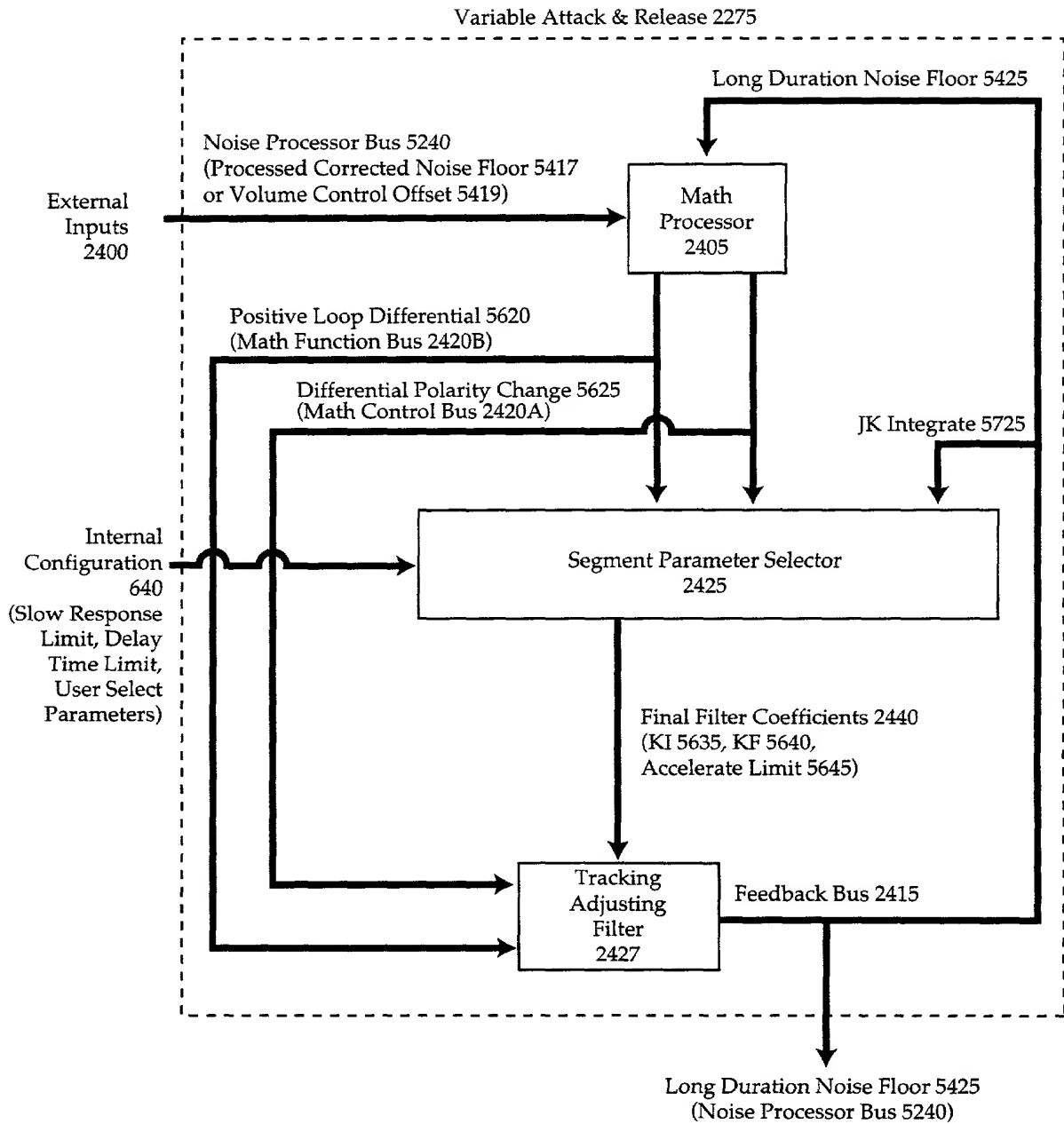


FIG. 55C

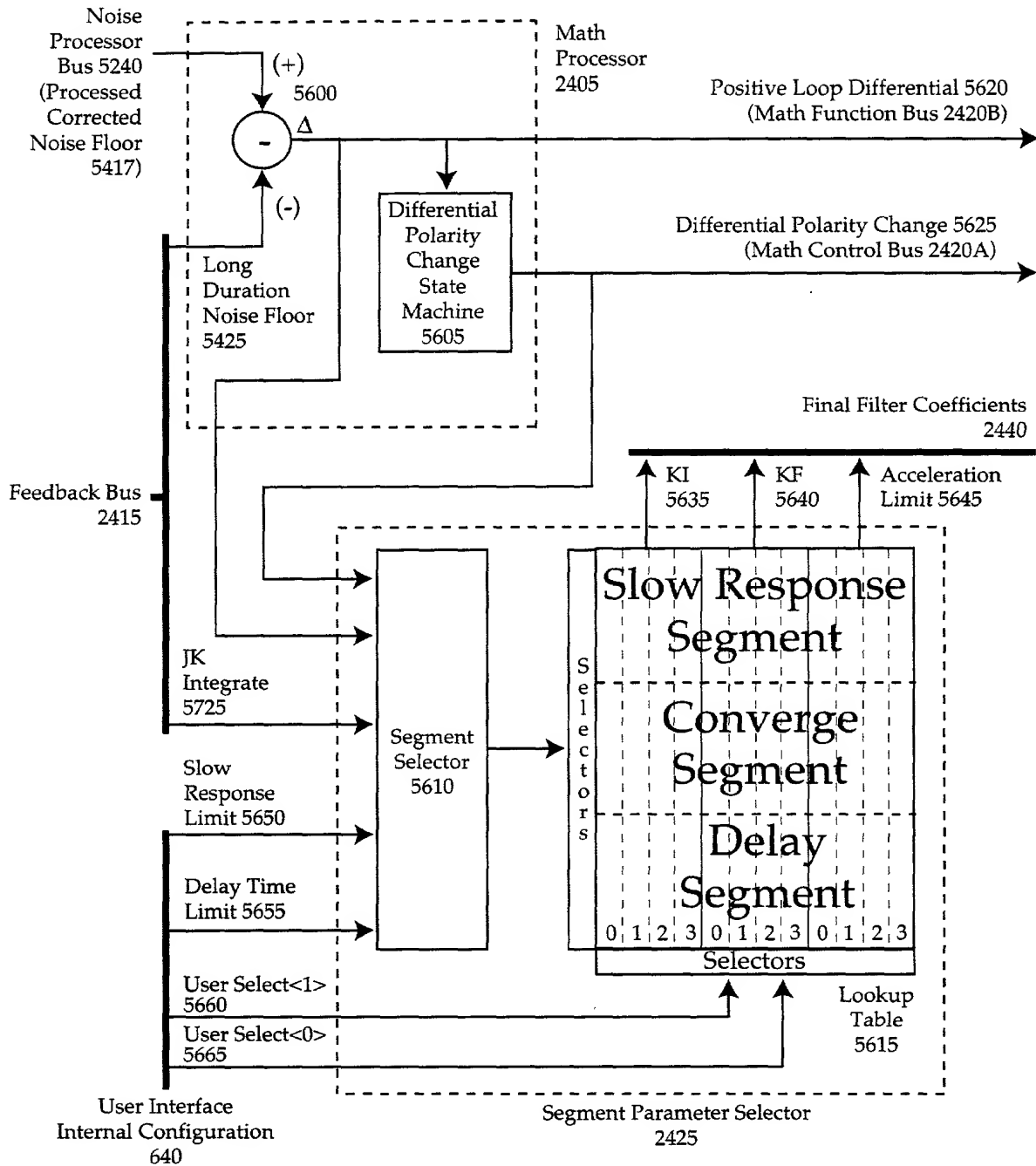


FIG. 56

The diagram illustrates the internal logic of the Acceleration Governor (5700). It features several input and output lines and internal processing blocks:

- Inputs:**
 - Final Filter Coefficients 2440:** Provides a signal to the Acceleration Limit 5645.
 - Acceleration Limit 5645:** Multiplied by the output of the Minimum Input Difference Selector (5717) at multiplier 5750.
 - KI 5635:** Multiplied by the Positive Loop Differential 5620 (Math Function Bus 2420B) at multiplier 5705.
 - KF 5640:** Multiplied by the output of the JK Integrate block (5725) at multiplier 5700.
 - JK Integrate 5725:** Provides a signal to the Clear input of the JK Integrate block (5725) and to multiplier 5700.
 - JK Hold 5745:** Provides a signal to the JK Hold input of the JK Integrate block (5725) and to the JK Hold input of the JK Hold block (5745).
 - Long Duration Noise Floor 5425 (Noise Processor Bus 5240):** Provides a signal to the Positive Loop Average block (5740).
- Internal Processing:**
 - The output of the Acceleration Limit 5645 is multiplied by the output of the Minimum Input Difference Selector (5717) at multiplier 5750.
 - The output of the Minimum Input Difference Selector (5717) is added to the output of the Positive Loop Average block (5740) at adder 5735.
 - The output of the Positive Loop Average block (5740) is added to the output of the JK Integrate block (5725) at adder 5735.
 - The output of the JK Integrate block (5725) is added to the output of the Positive Loop Average block (5740) at adder 5735.
 - The output of the JK Integrate block (5725) is multiplied by the output of the Positive Loop Average block (5740) at multiplier 5700.
 - The output of the Positive Loop Average block (5740) is multiplied by the output of the Positive Loop Average block (5740) at multiplier 5705.
 - The output of the Positive Loop Average block (5740) is added to the output of the Positive Loop Average block (5740) at adder 5710.
 - The output of the Positive Loop Average block (5740) is added to the output of the Positive Loop Average block (5740) at adder 5715.
 - The output of the Positive Loop Average block (5740) is added to the output of the Positive Loop Average block (5740) at adder 5720.
- Outputs:**
 - Feedback Bus 2415:** Receives signals from the JK Integrate 5725, JK Hold 5745, and the Positive Loop Average 5740.

Note: JK Hold is a positive bias value.

FIG. 57A

FIG. 57A

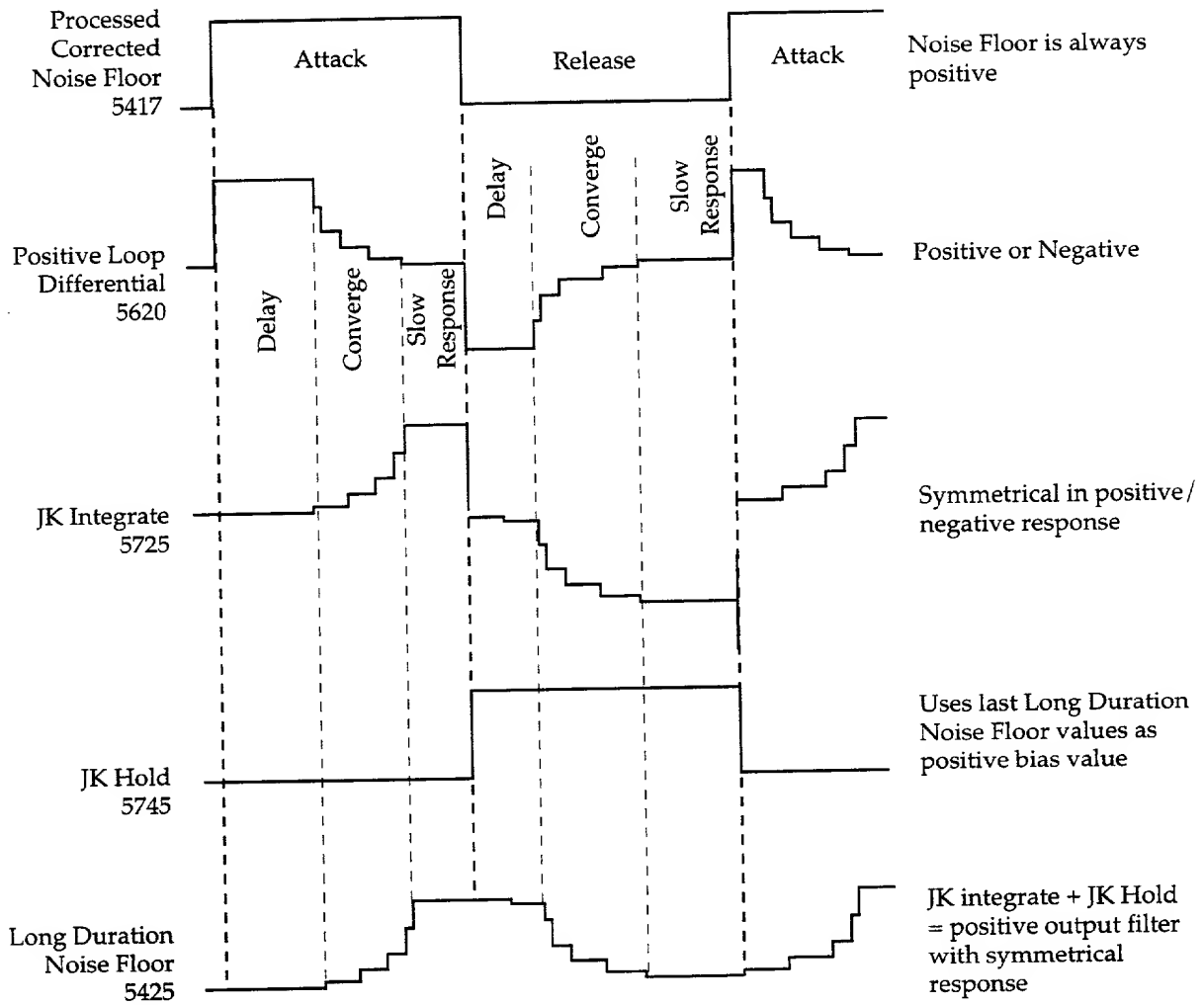


FIG. 57B

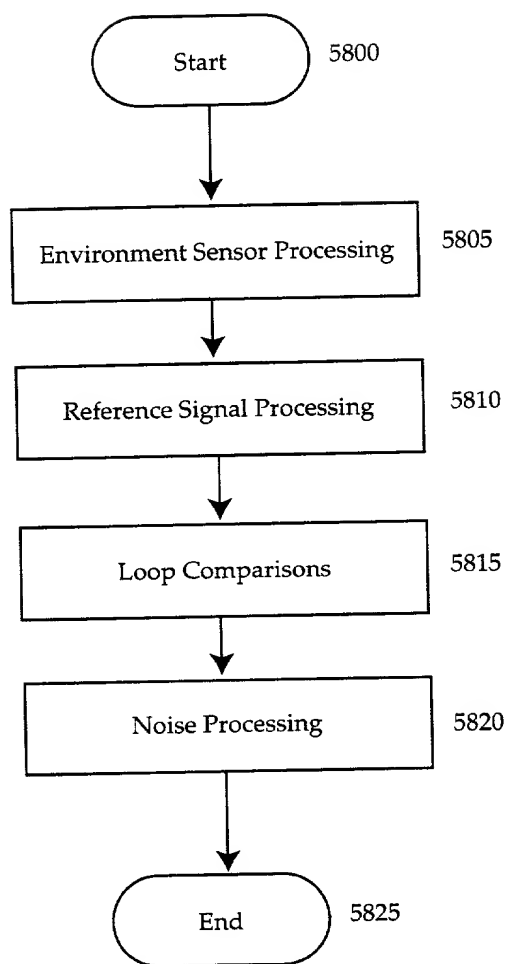


FIG. 58

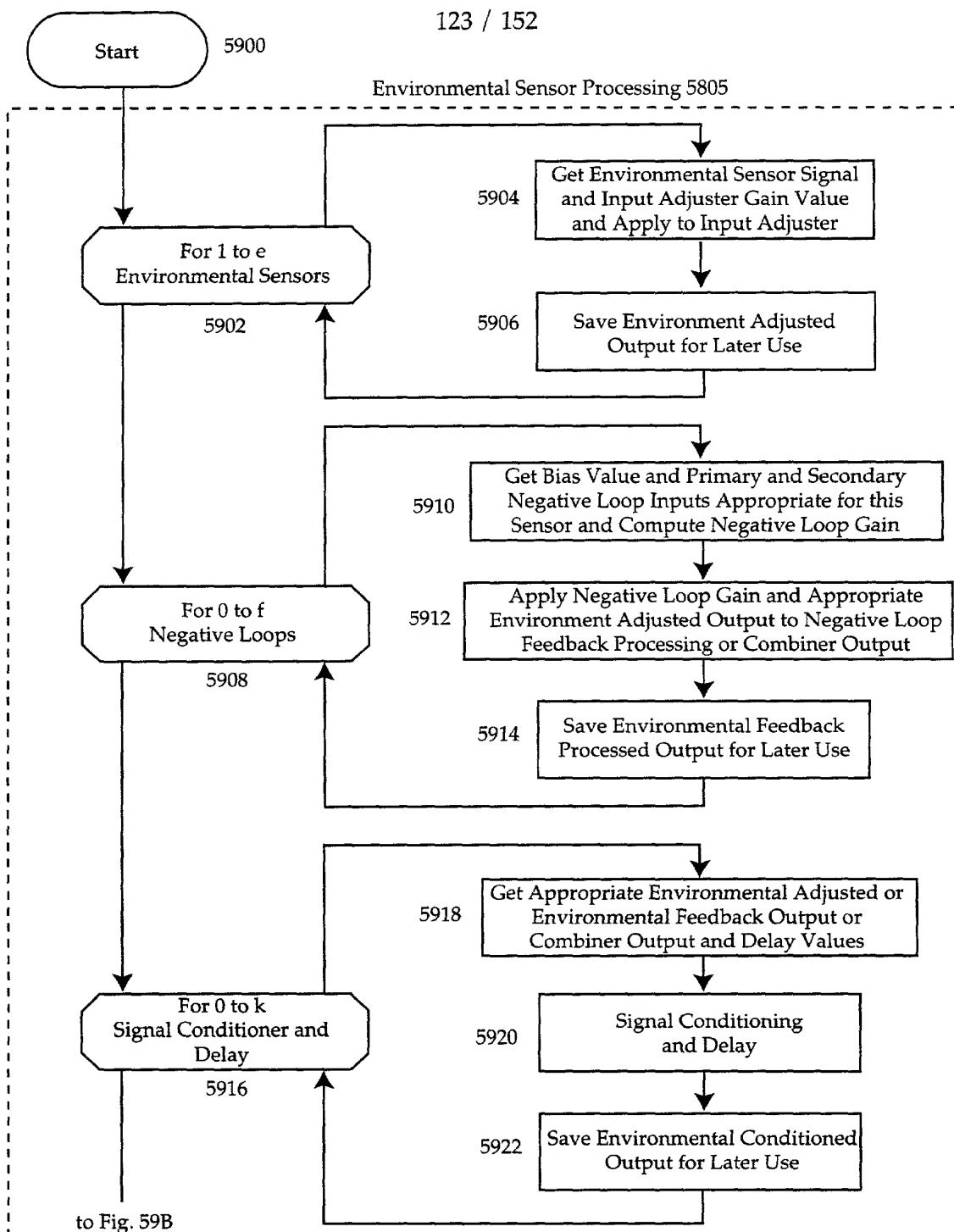


FIG. 59A

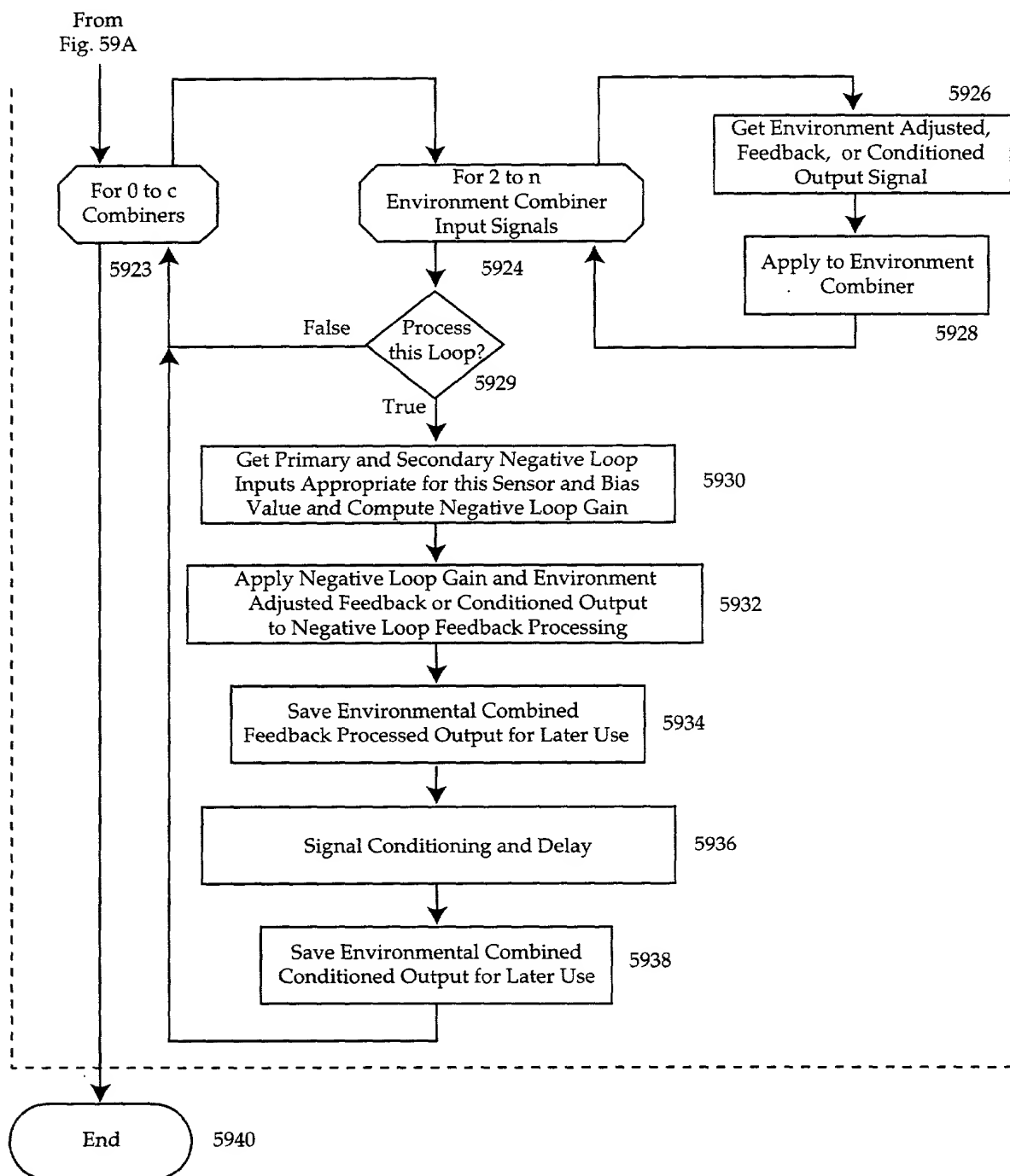


FIG. 59B

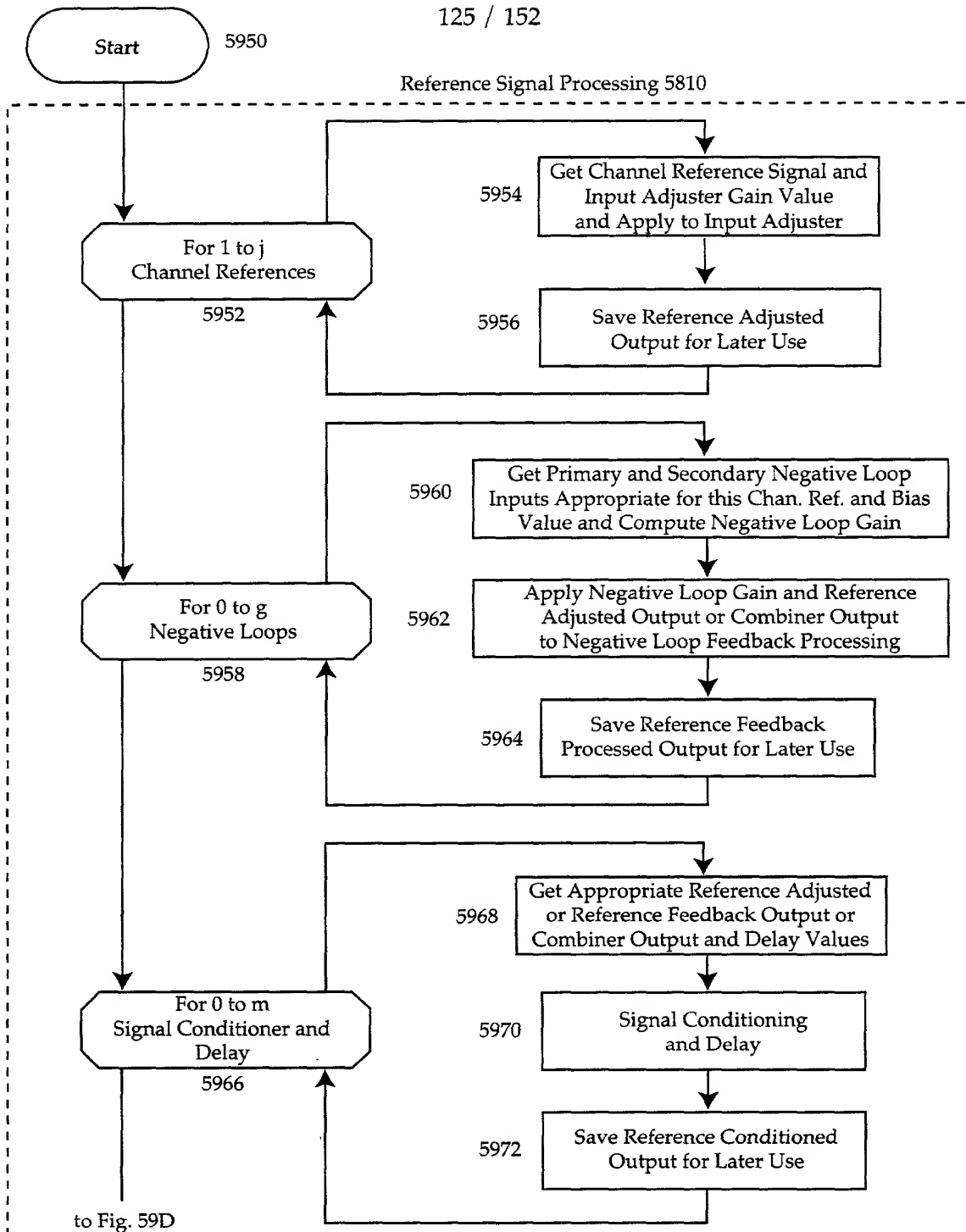


FIG. 59C

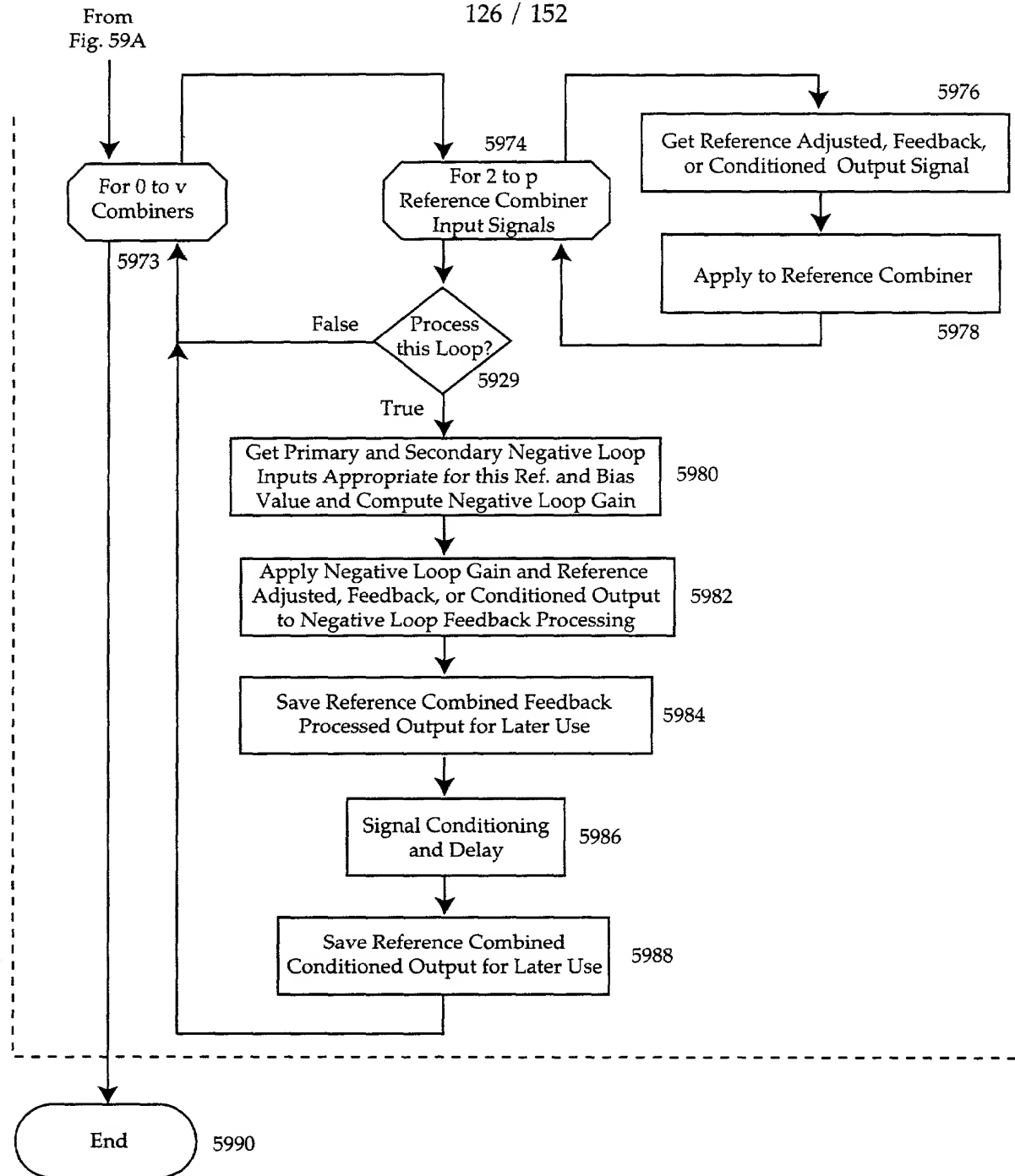


FIG. 59D

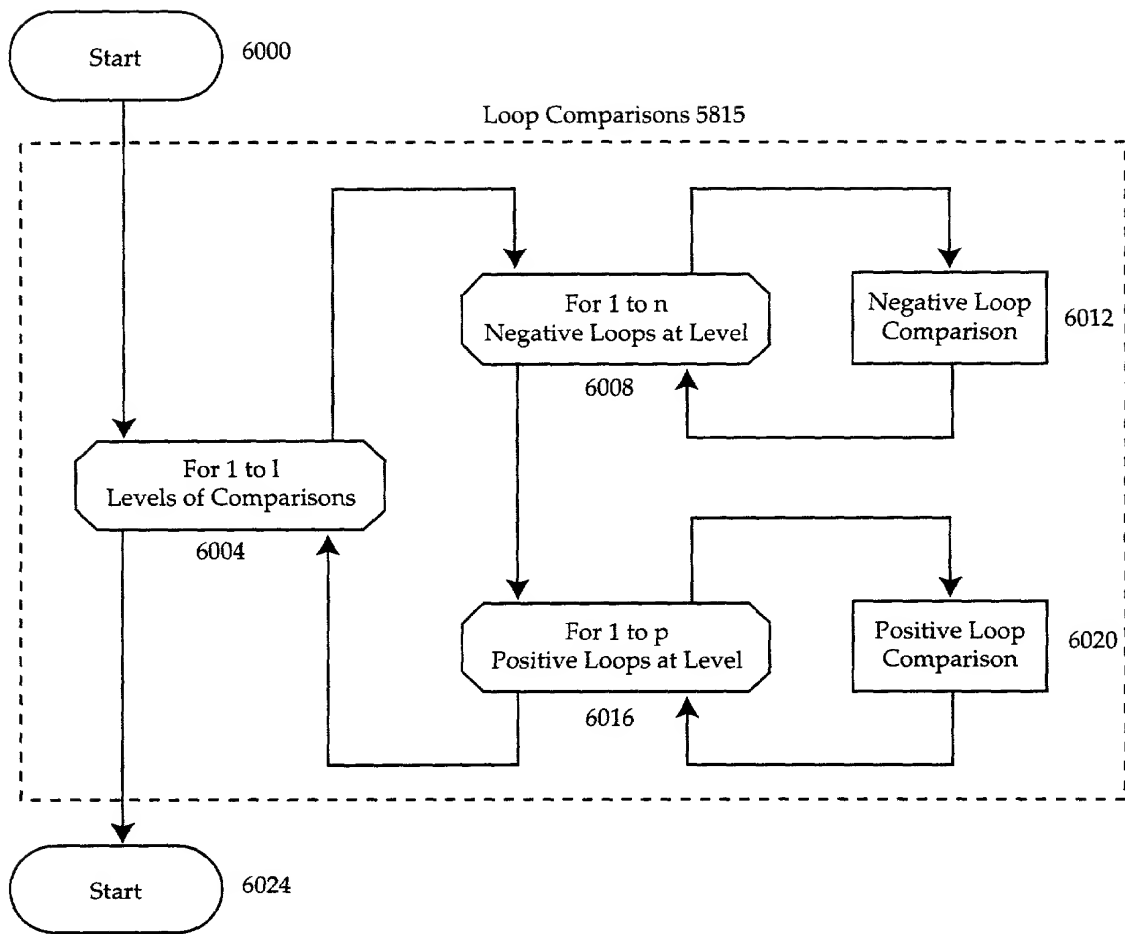


FIG. 60A

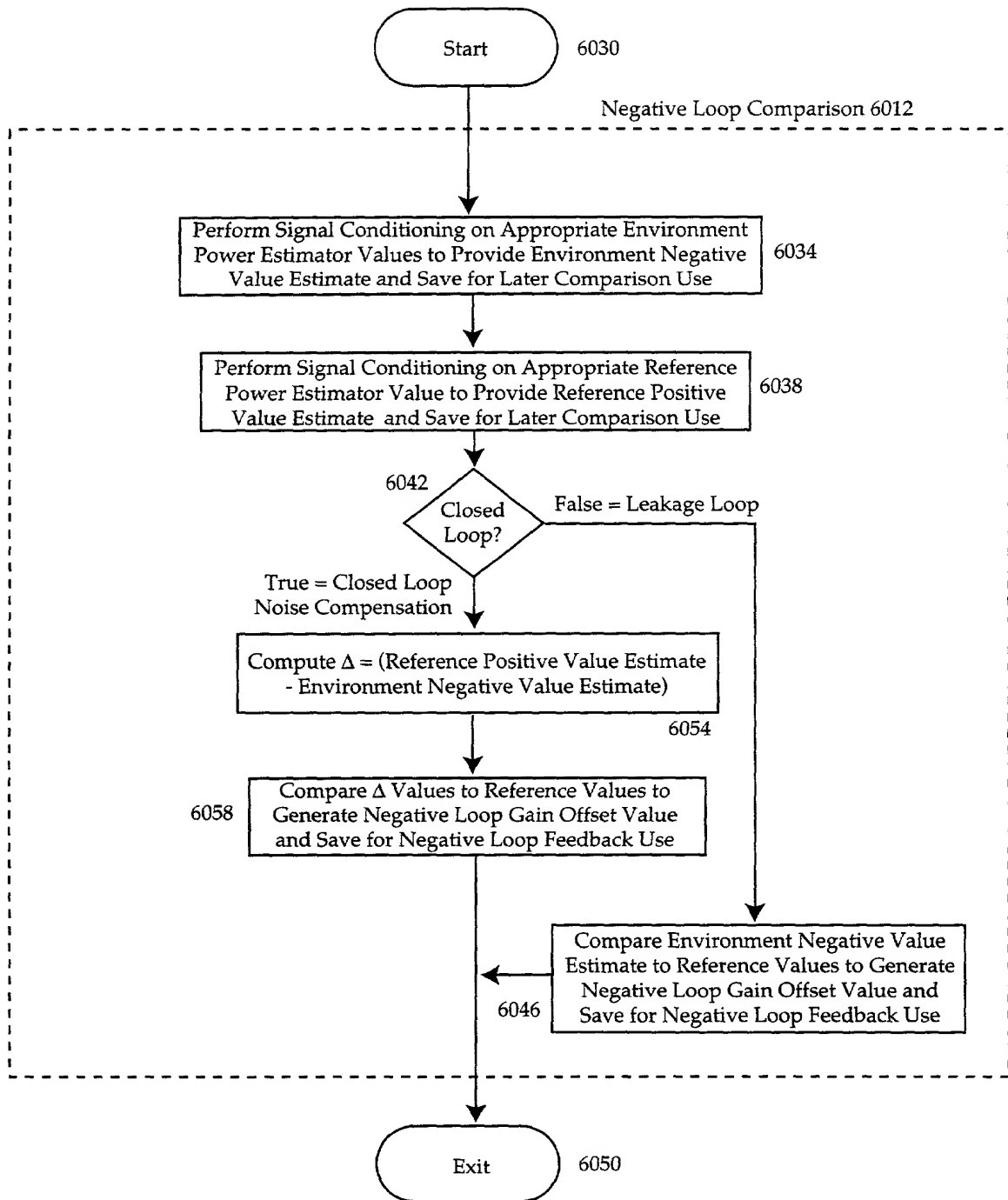


FIG. 60B

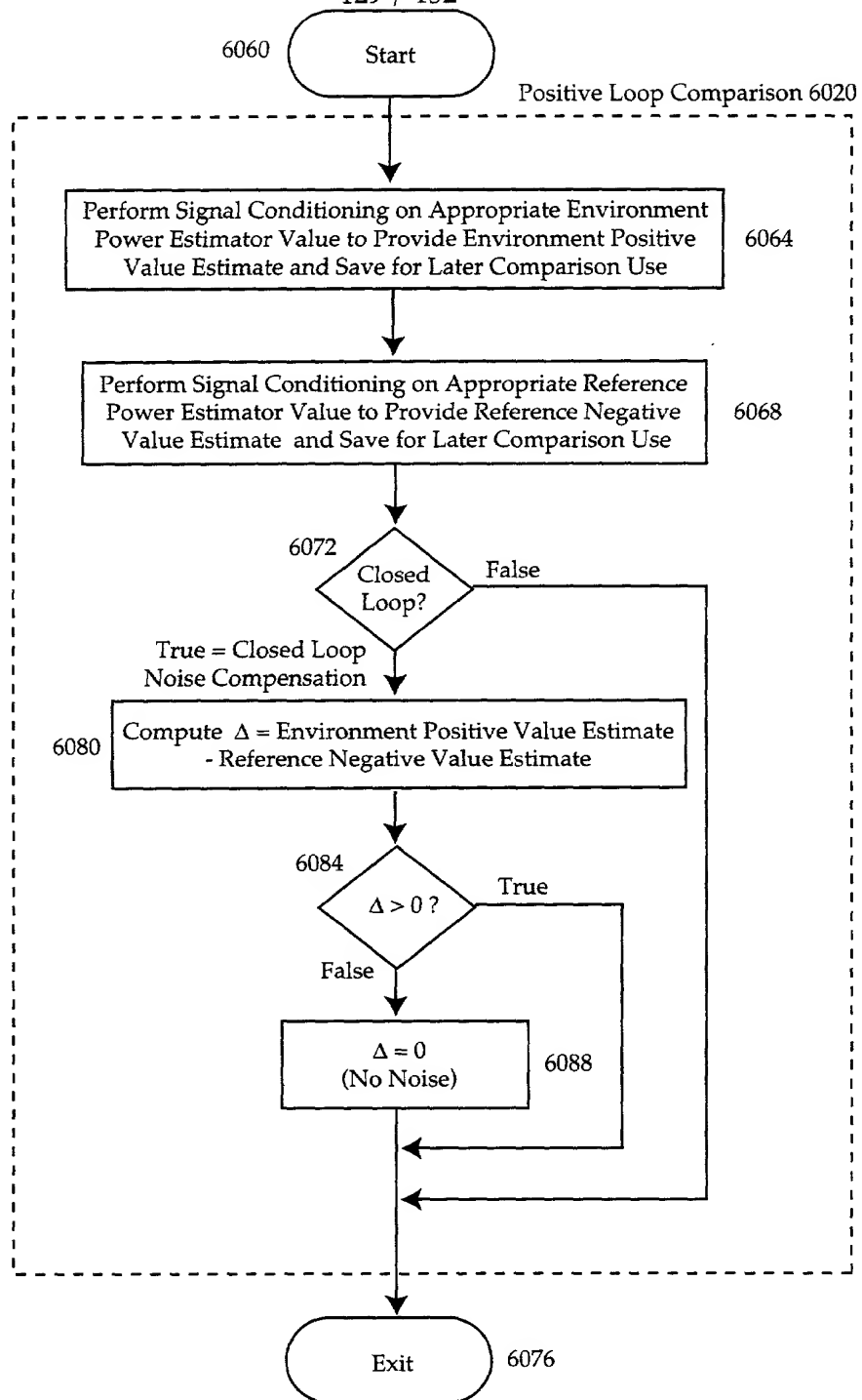


FIG. 60C

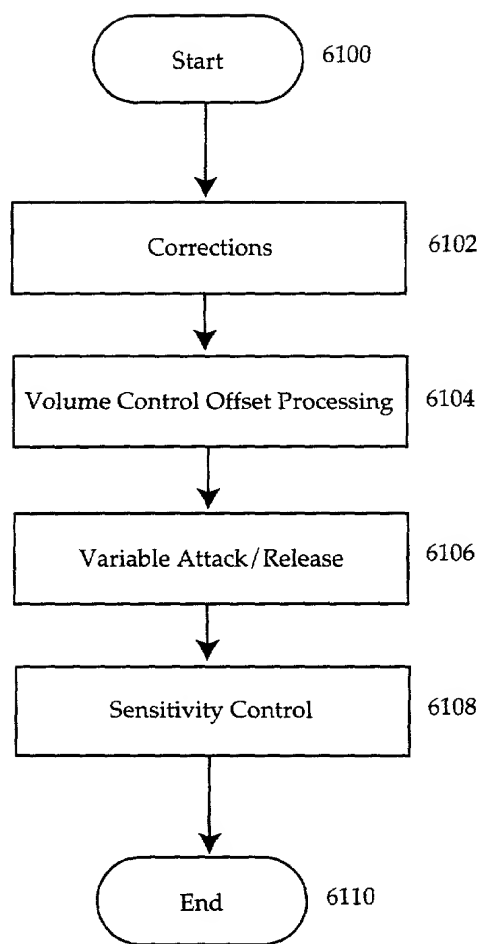


FIG. 61A

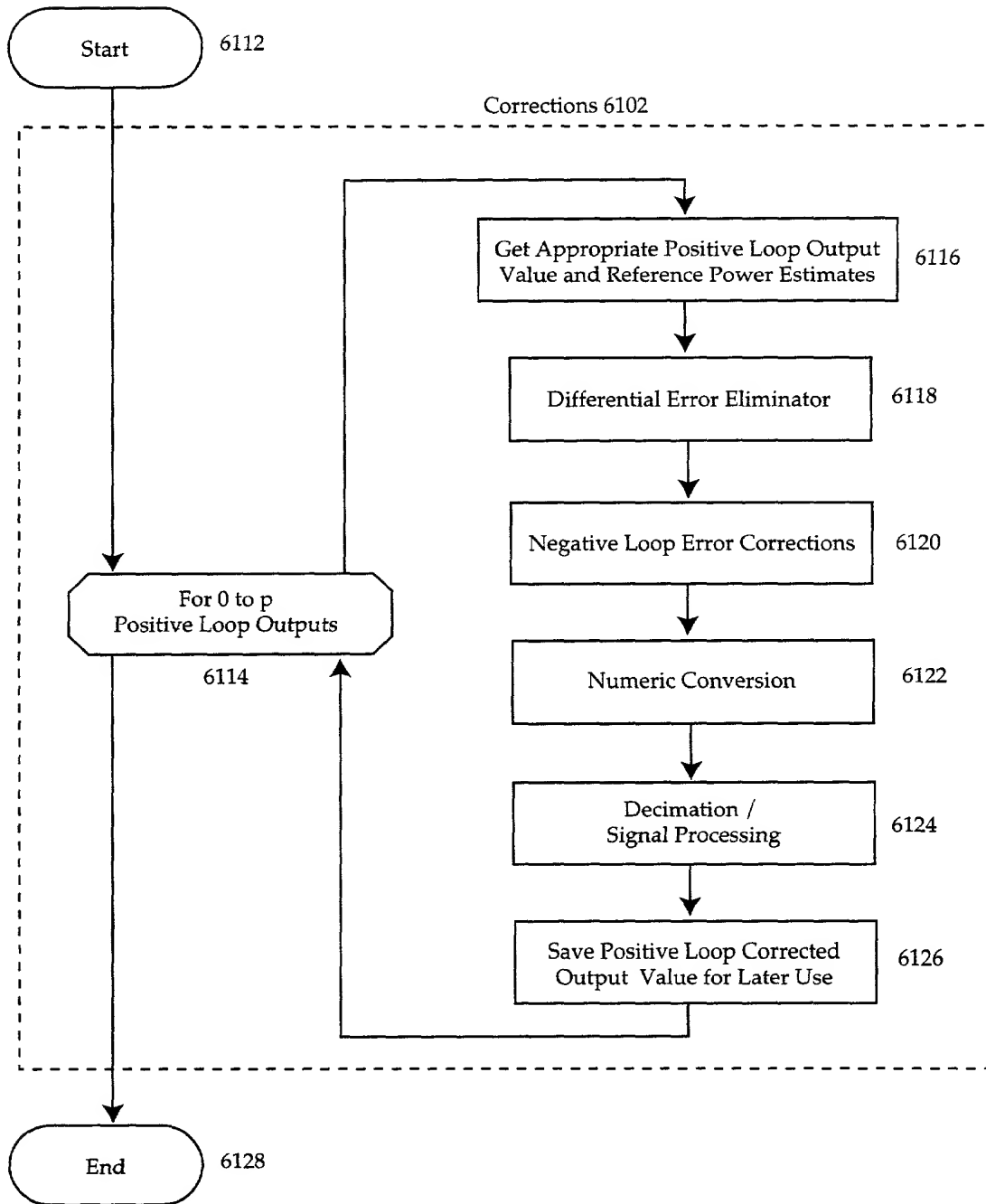


FIG. 61B

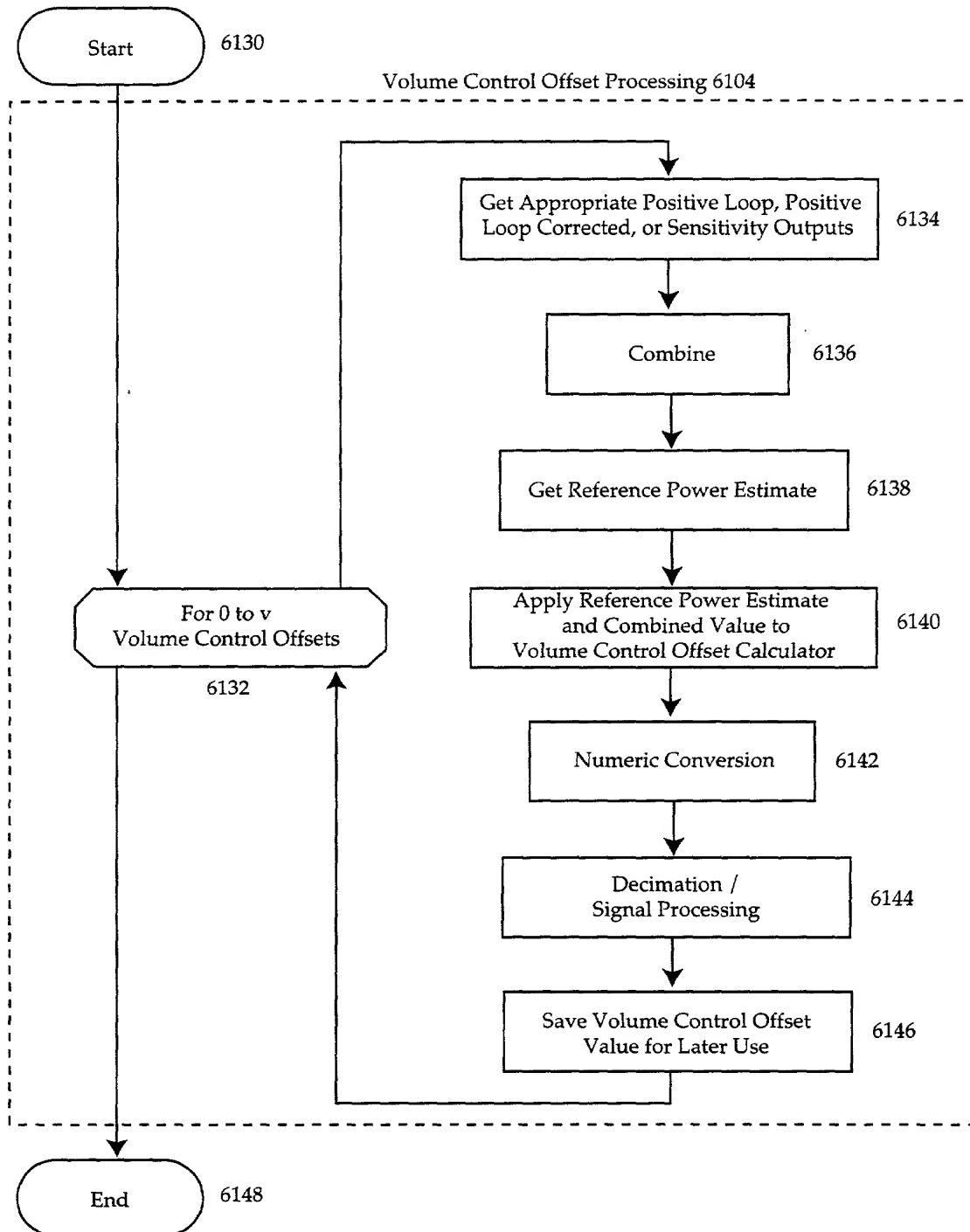


FIG. 61C

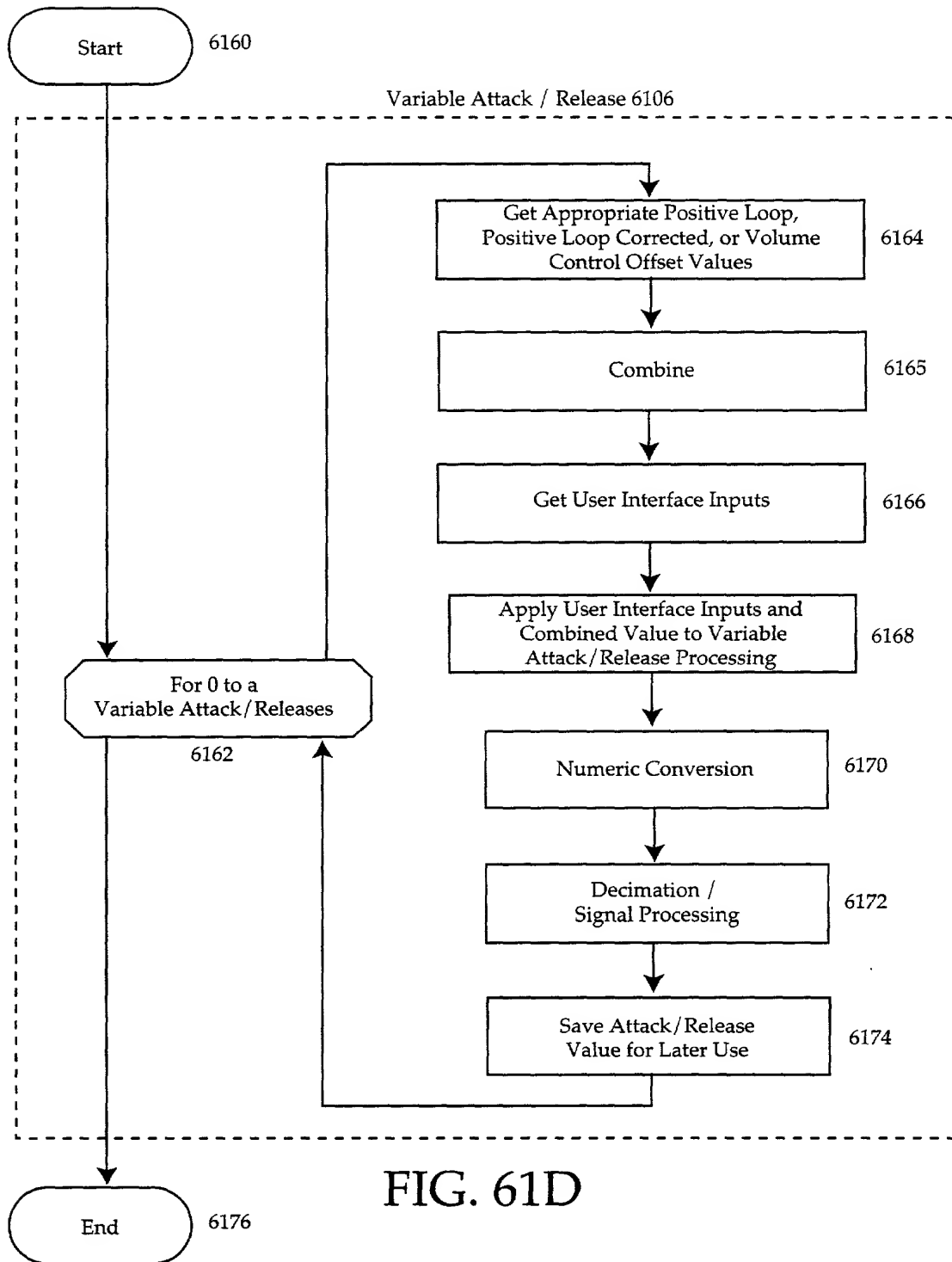


FIG. 61D

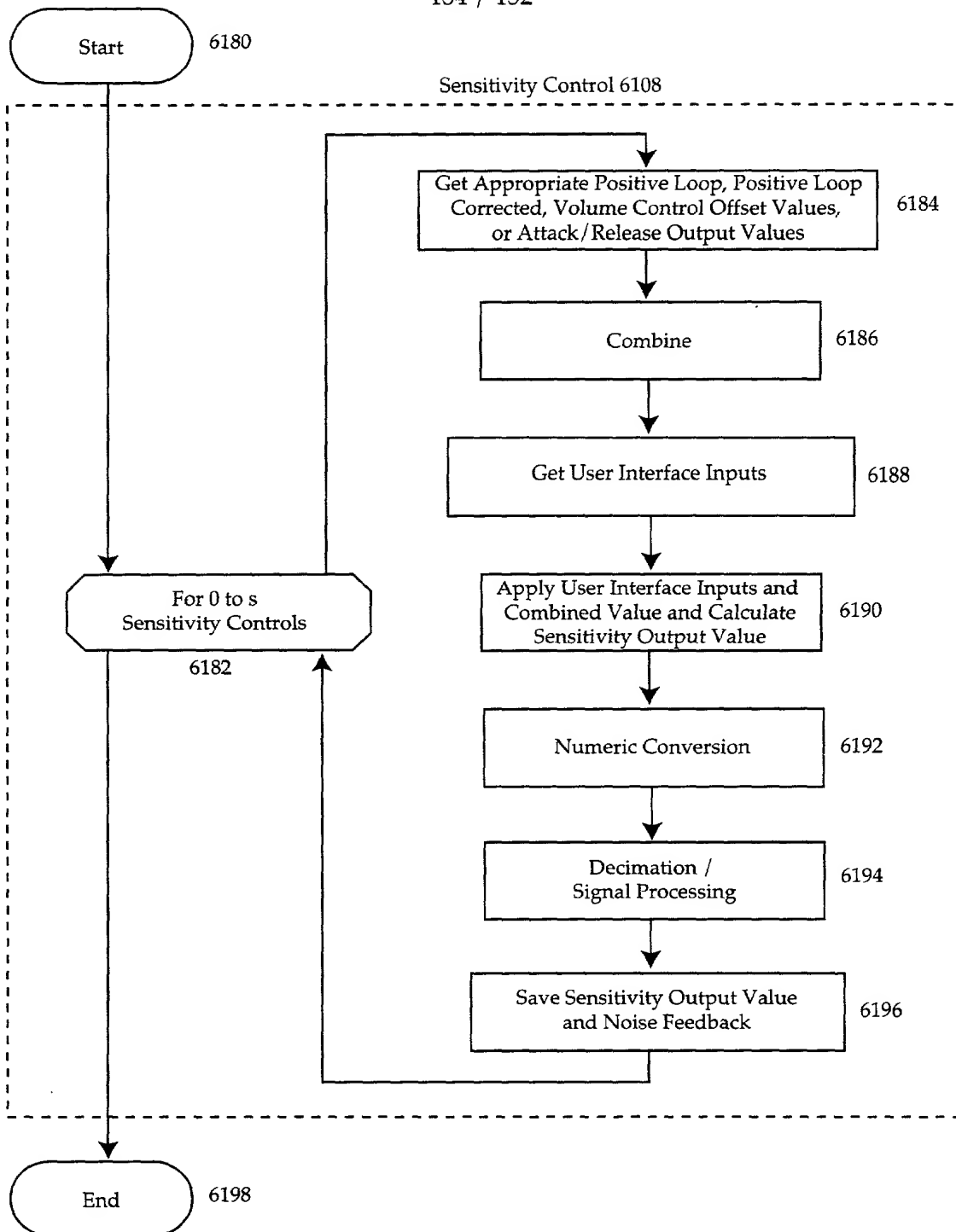
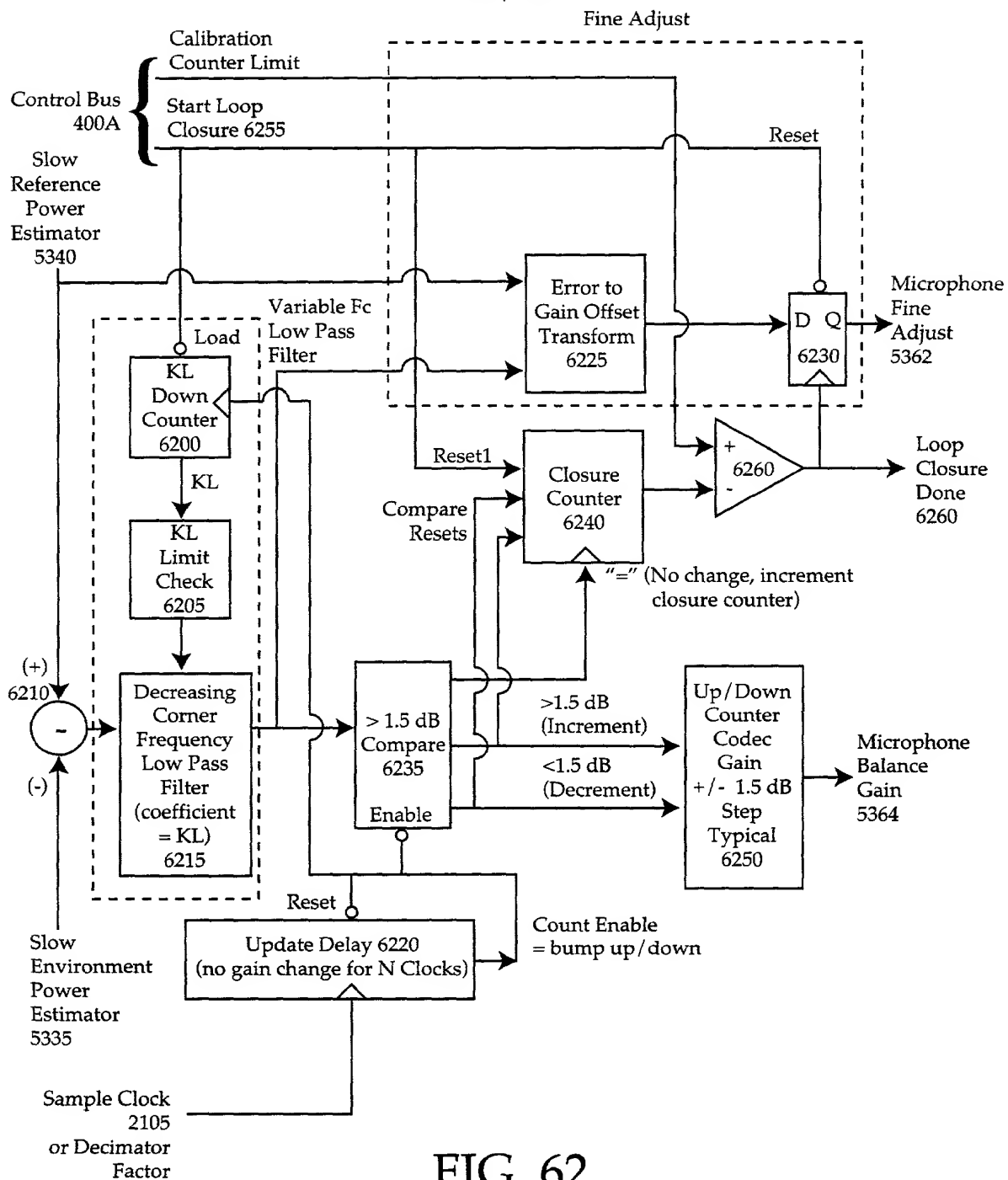


FIG. 61E



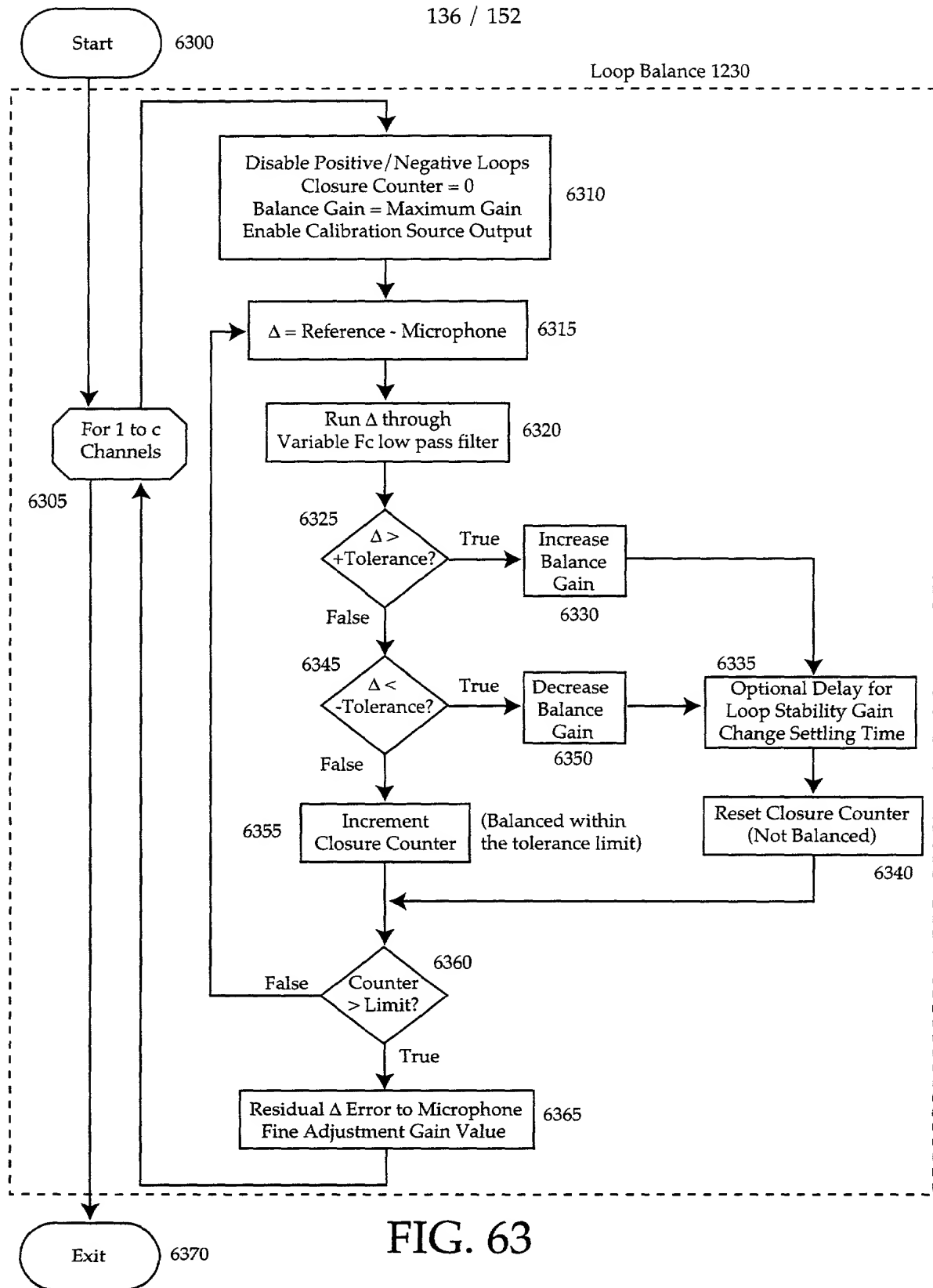


FIG. 63

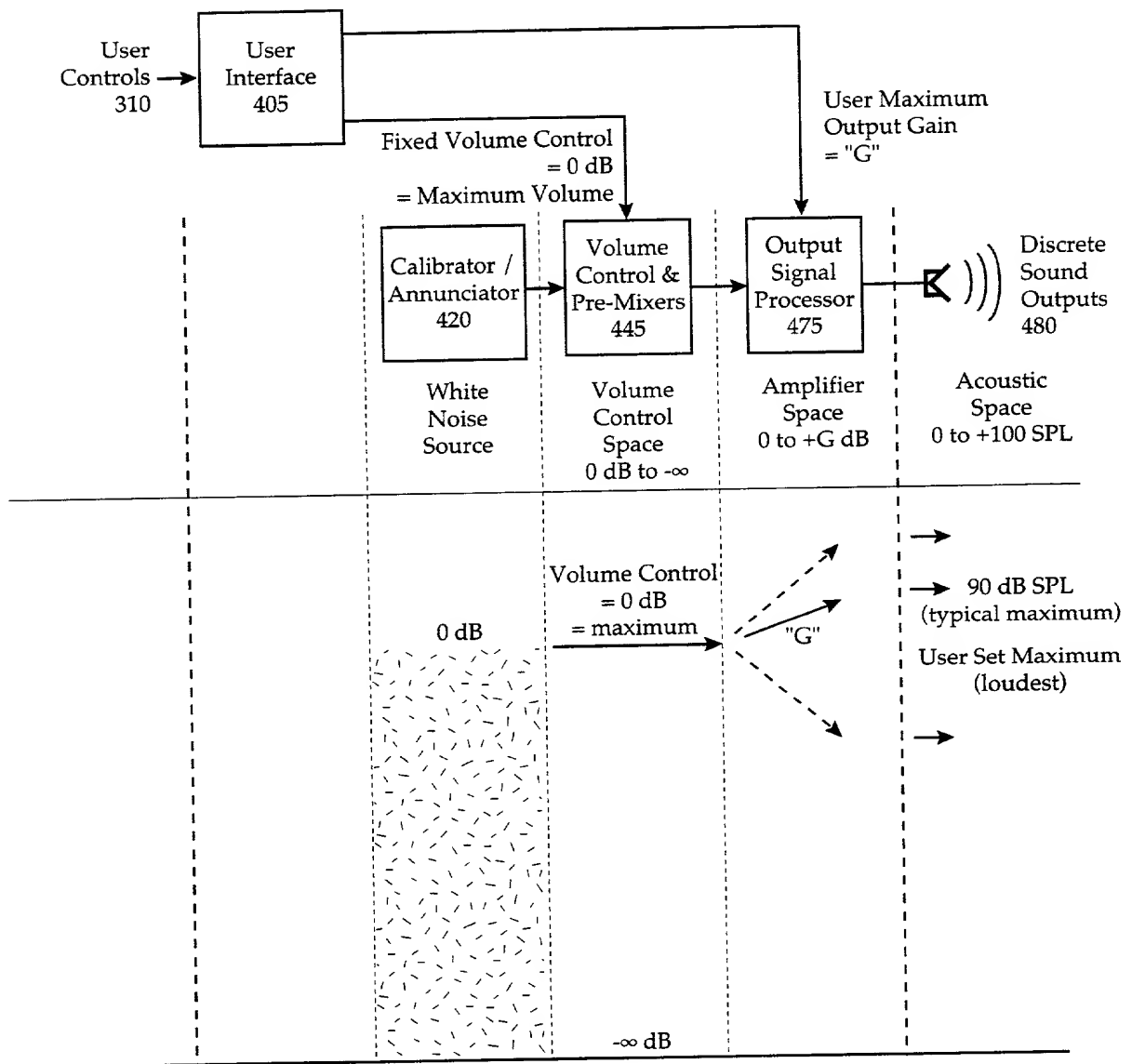


FIG. 64

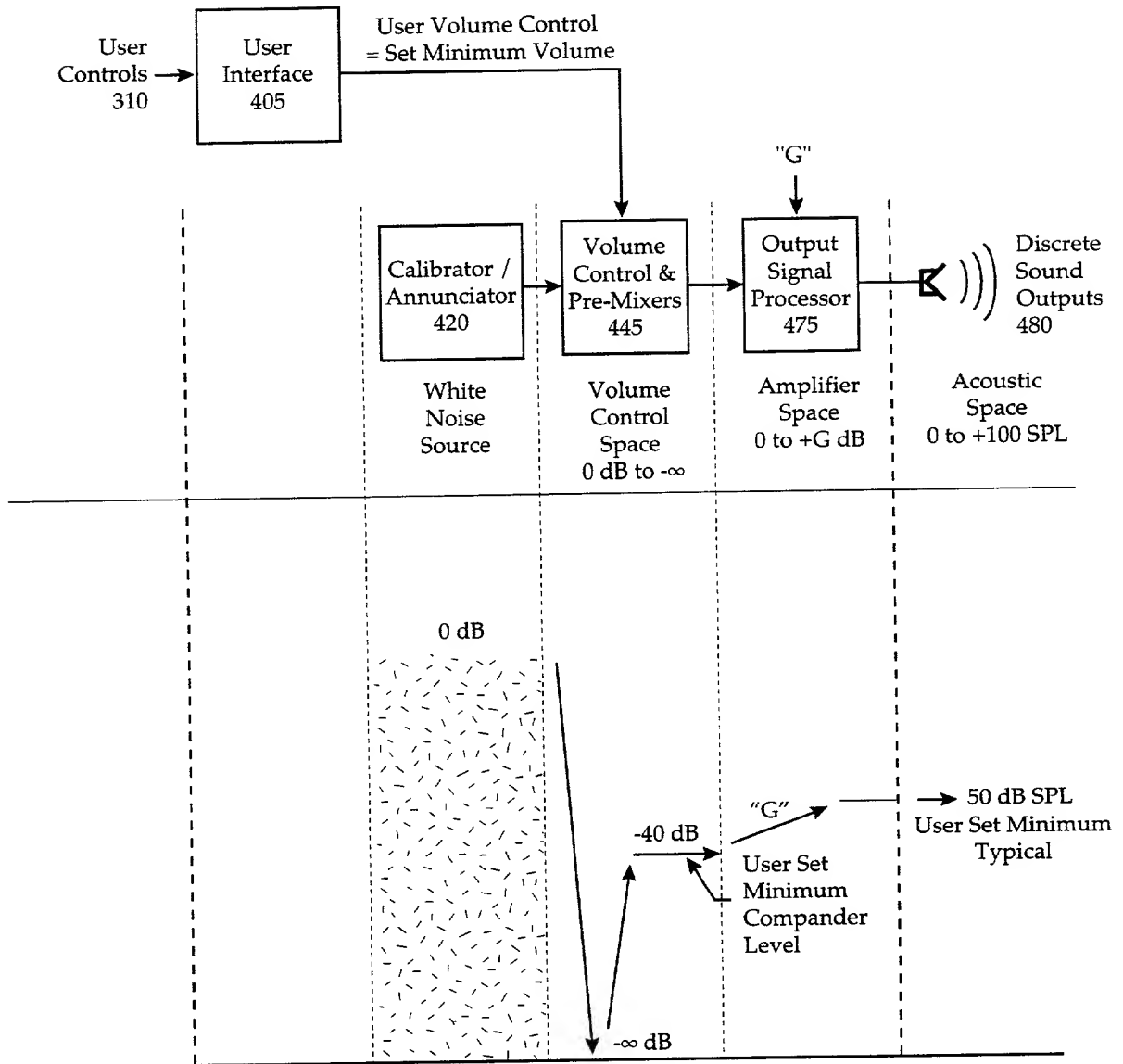


FIG. 65

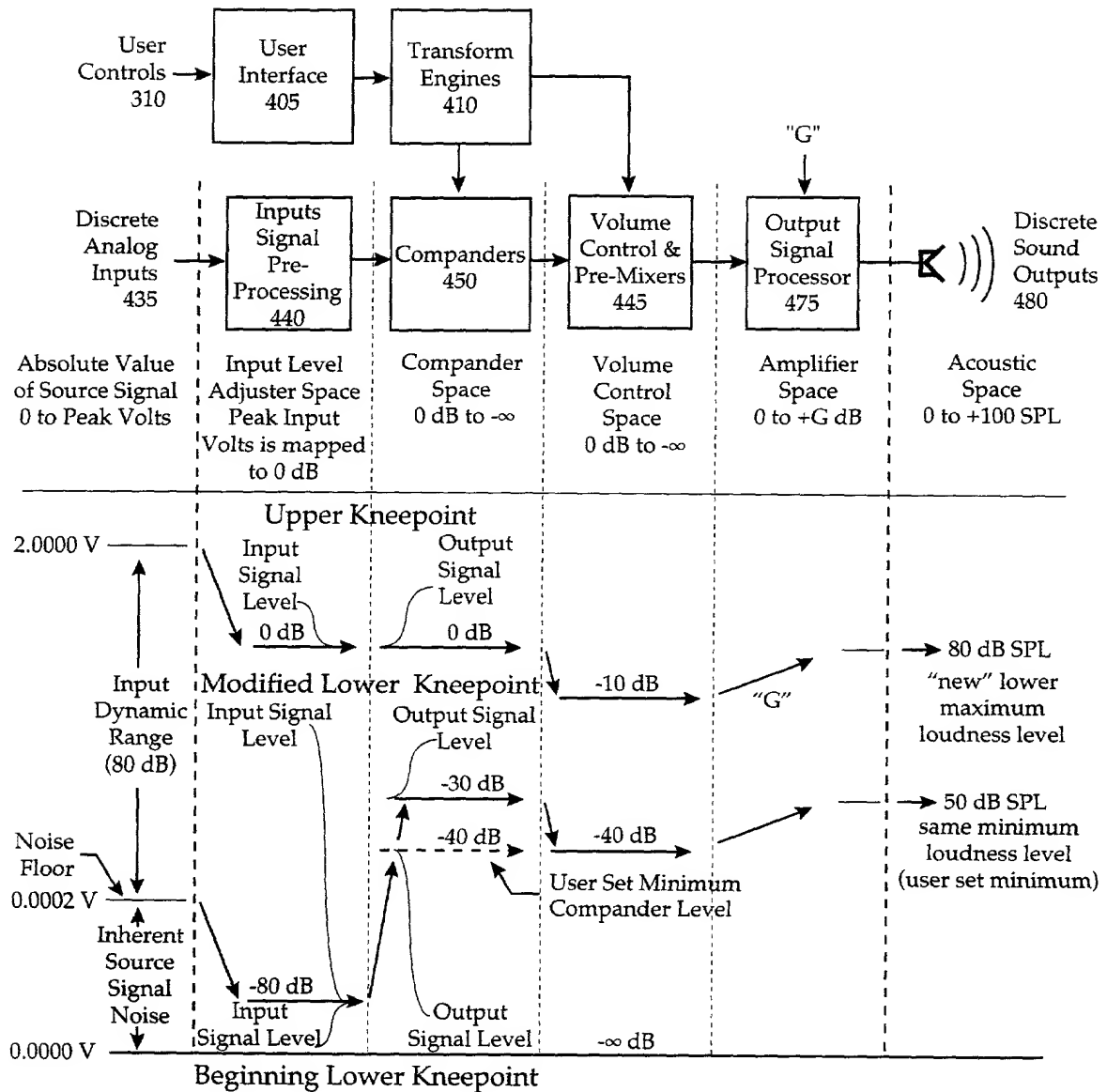


FIG. 66

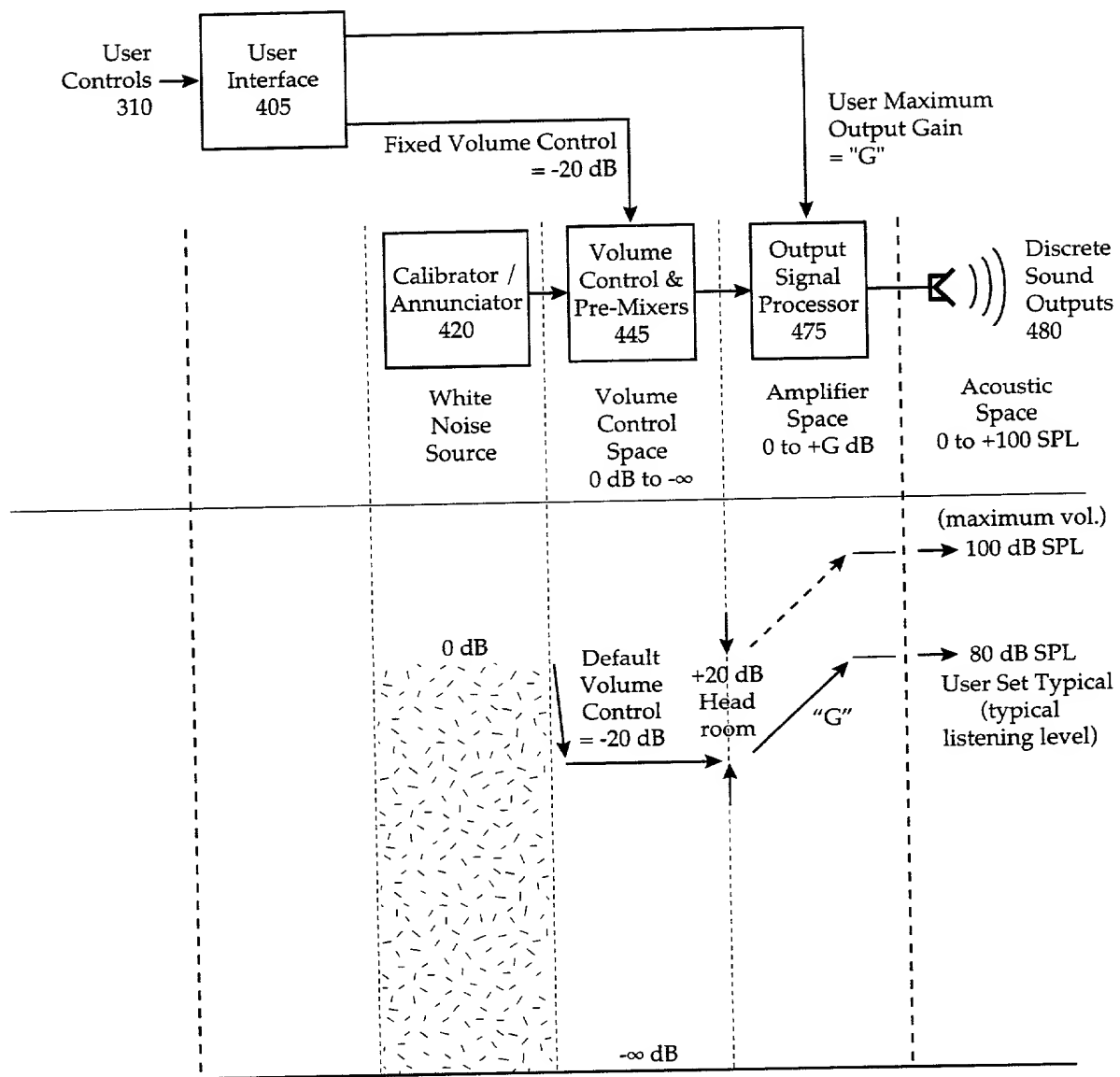


FIG. 67

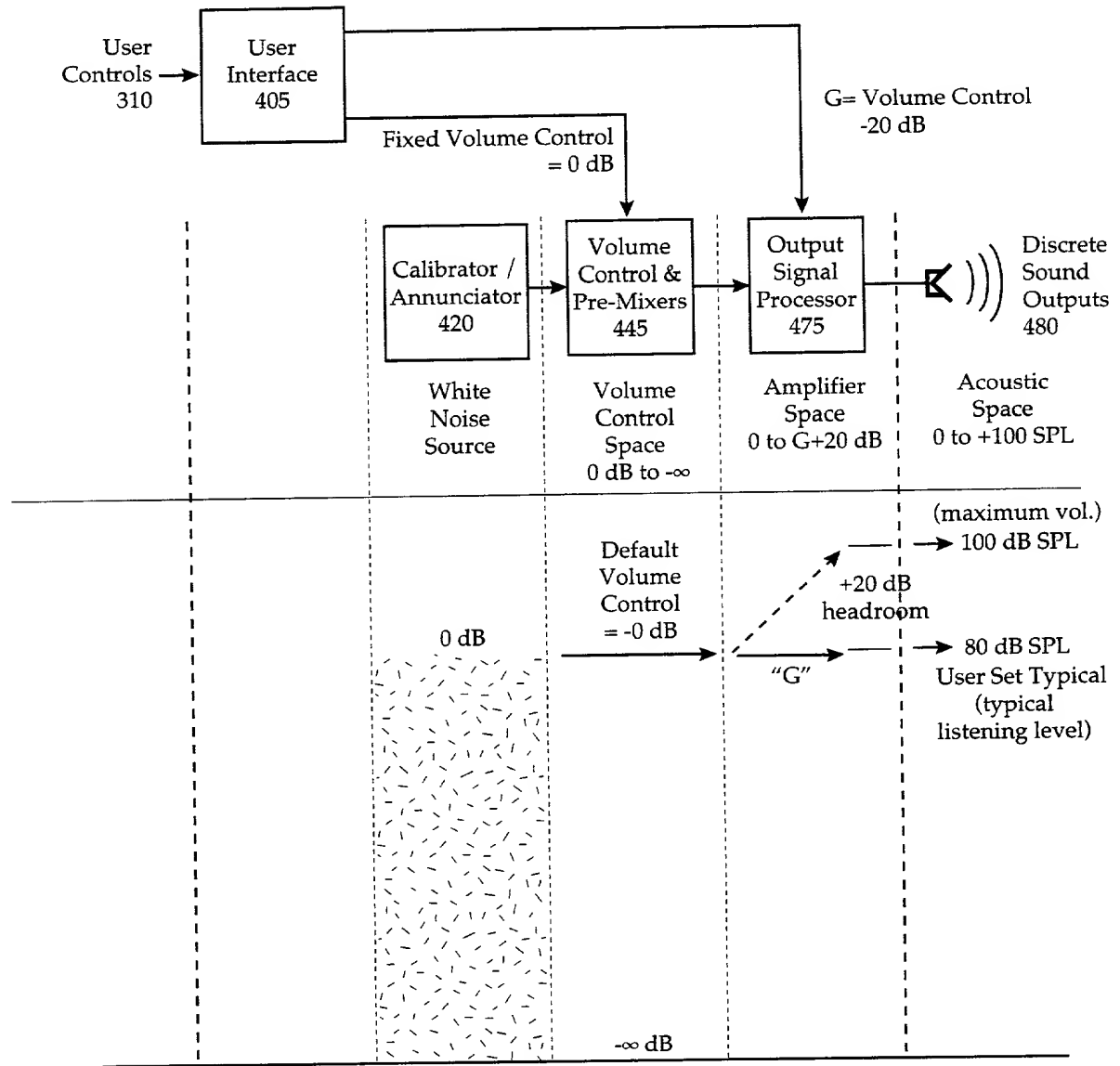


FIG. 68

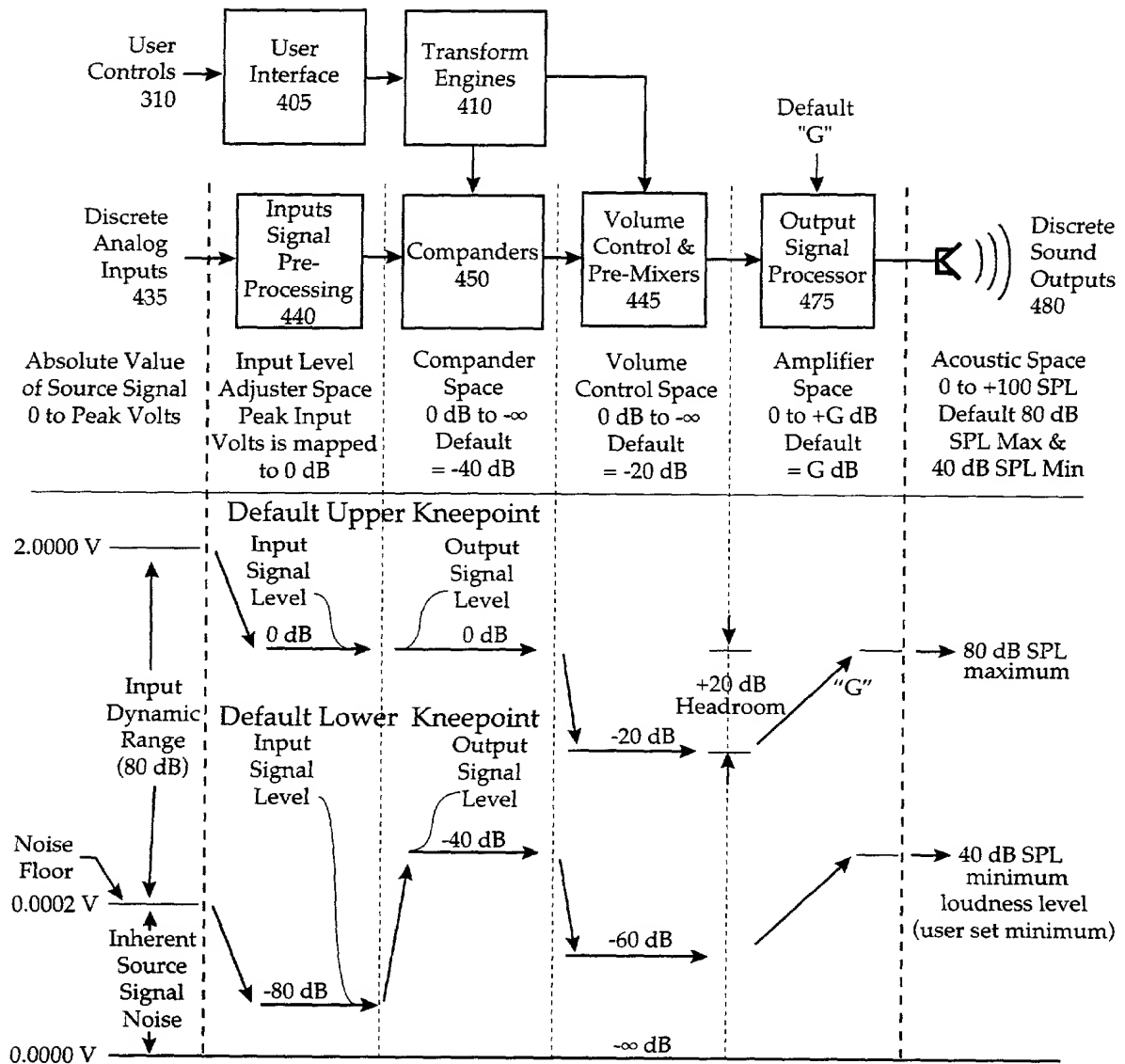


FIG. 69

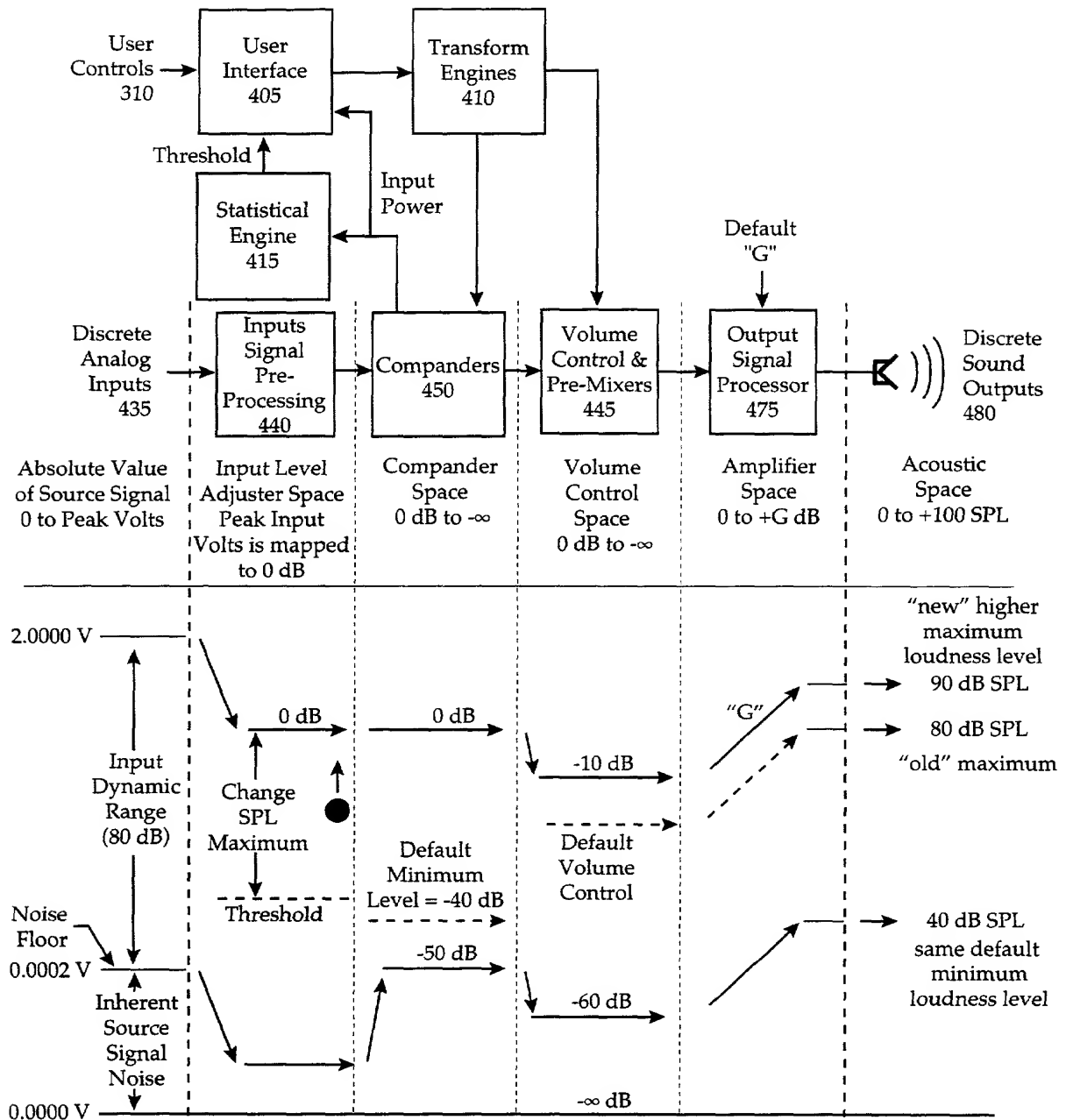


FIG. 70

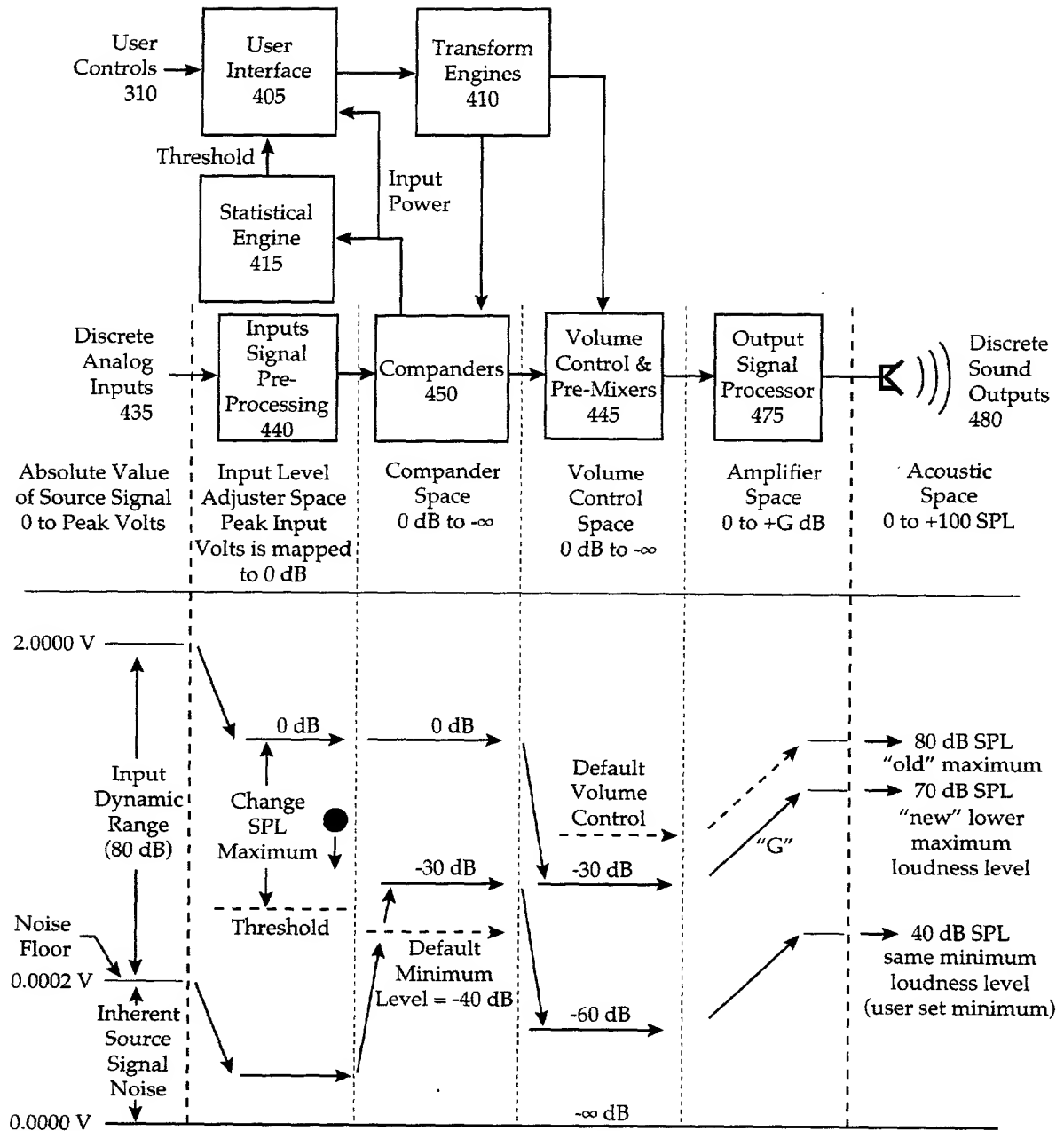


FIG. 71

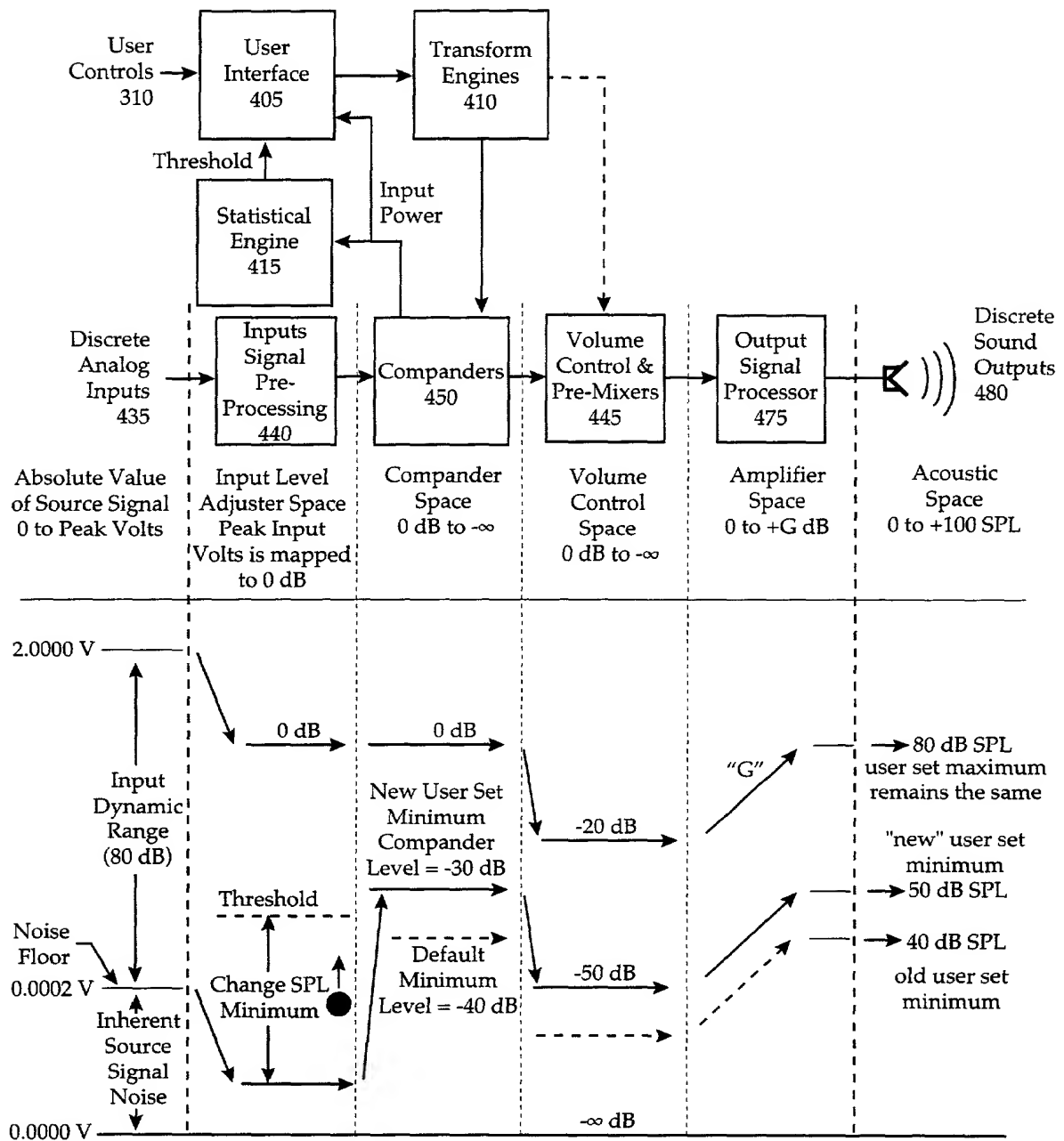


FIG. 72

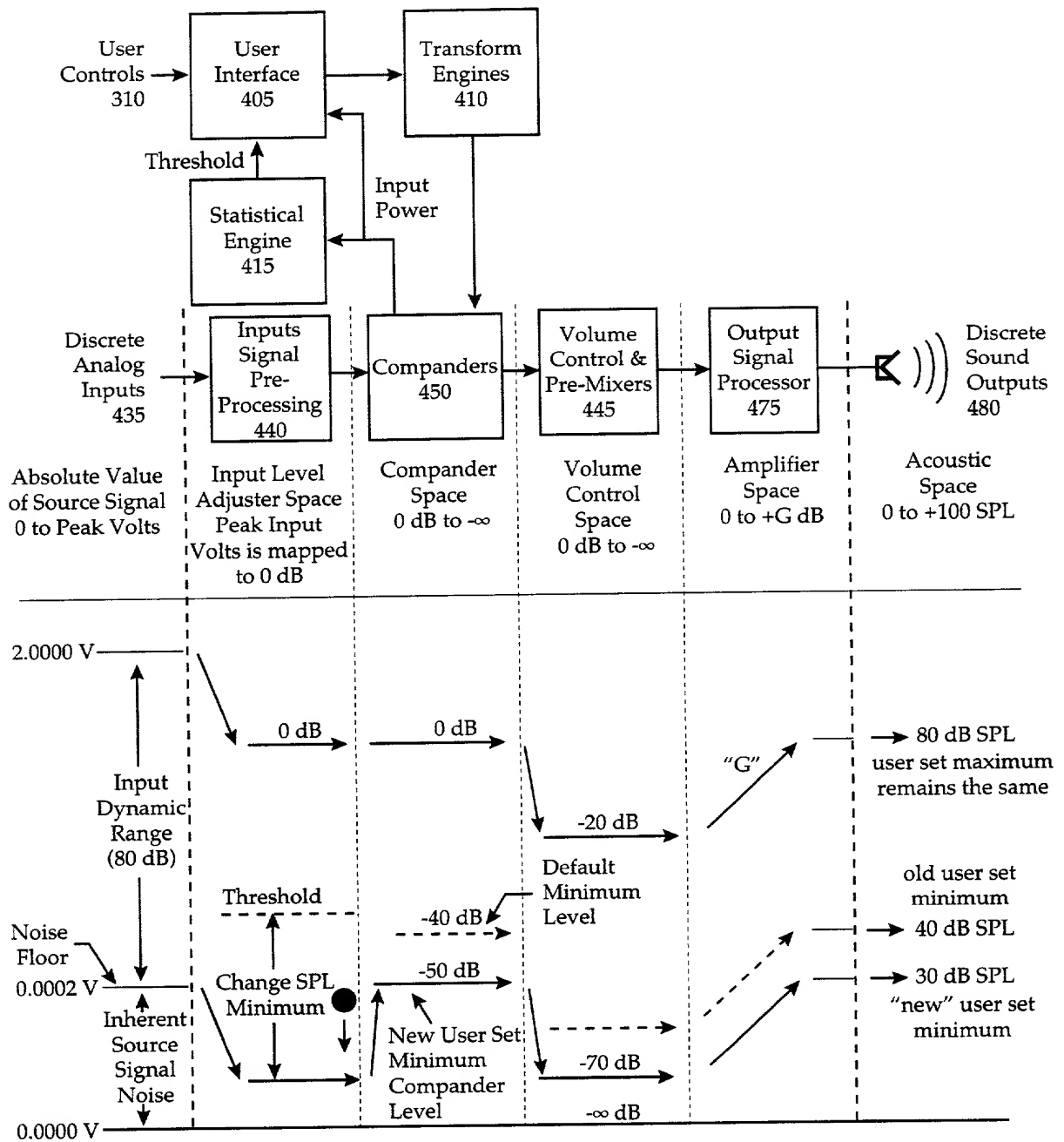


FIG. 73

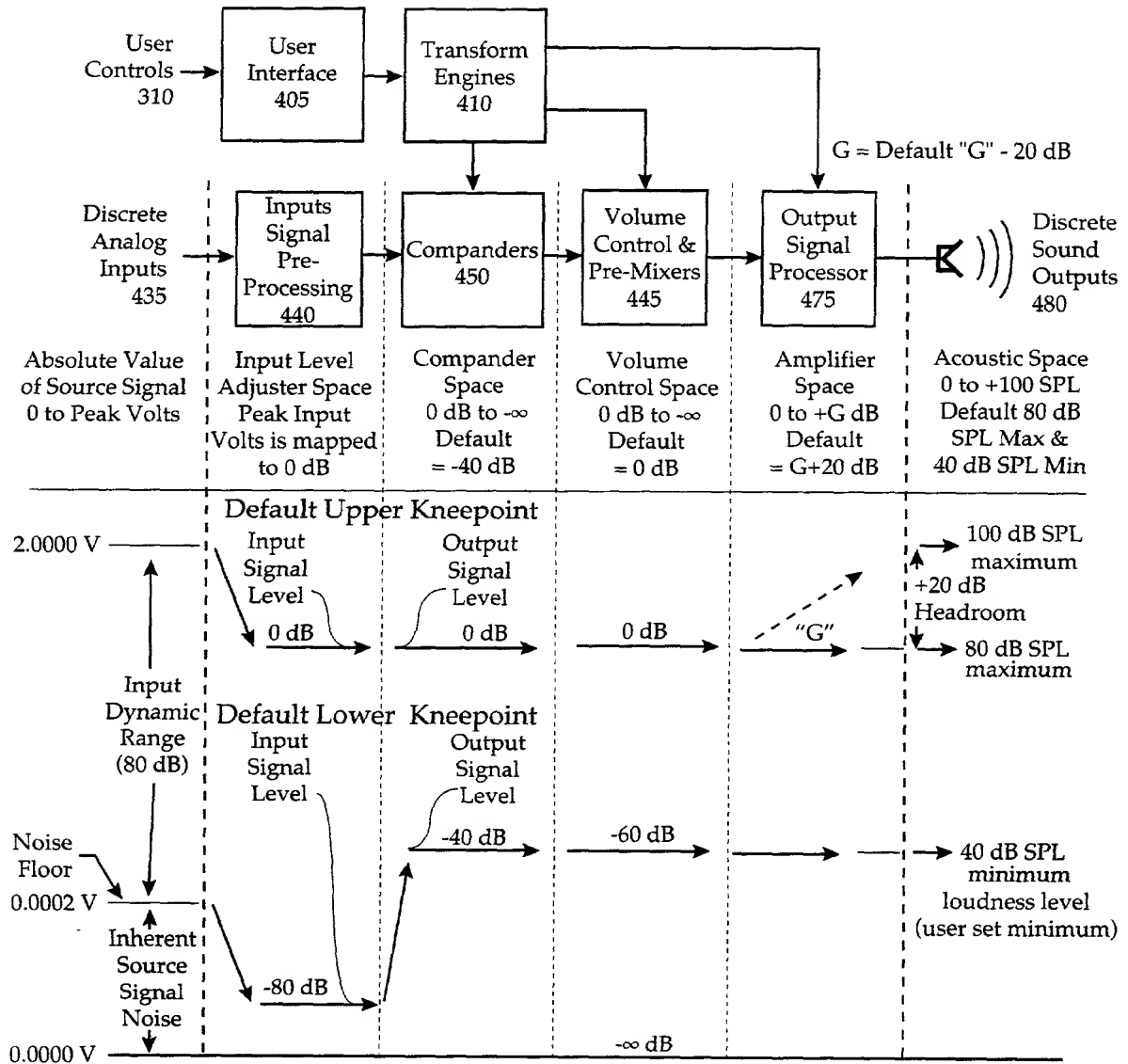


FIG. 74

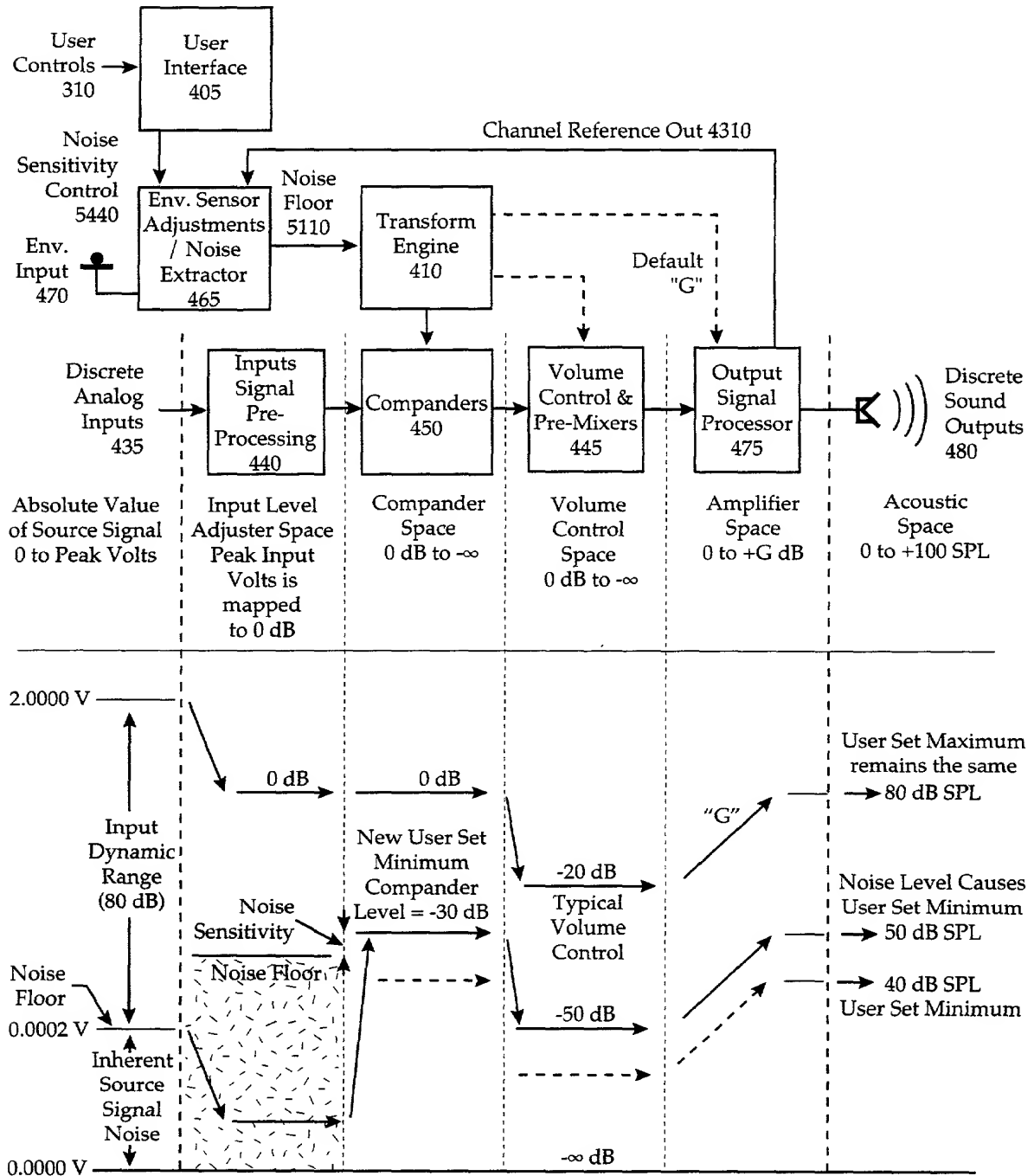


FIG. 75

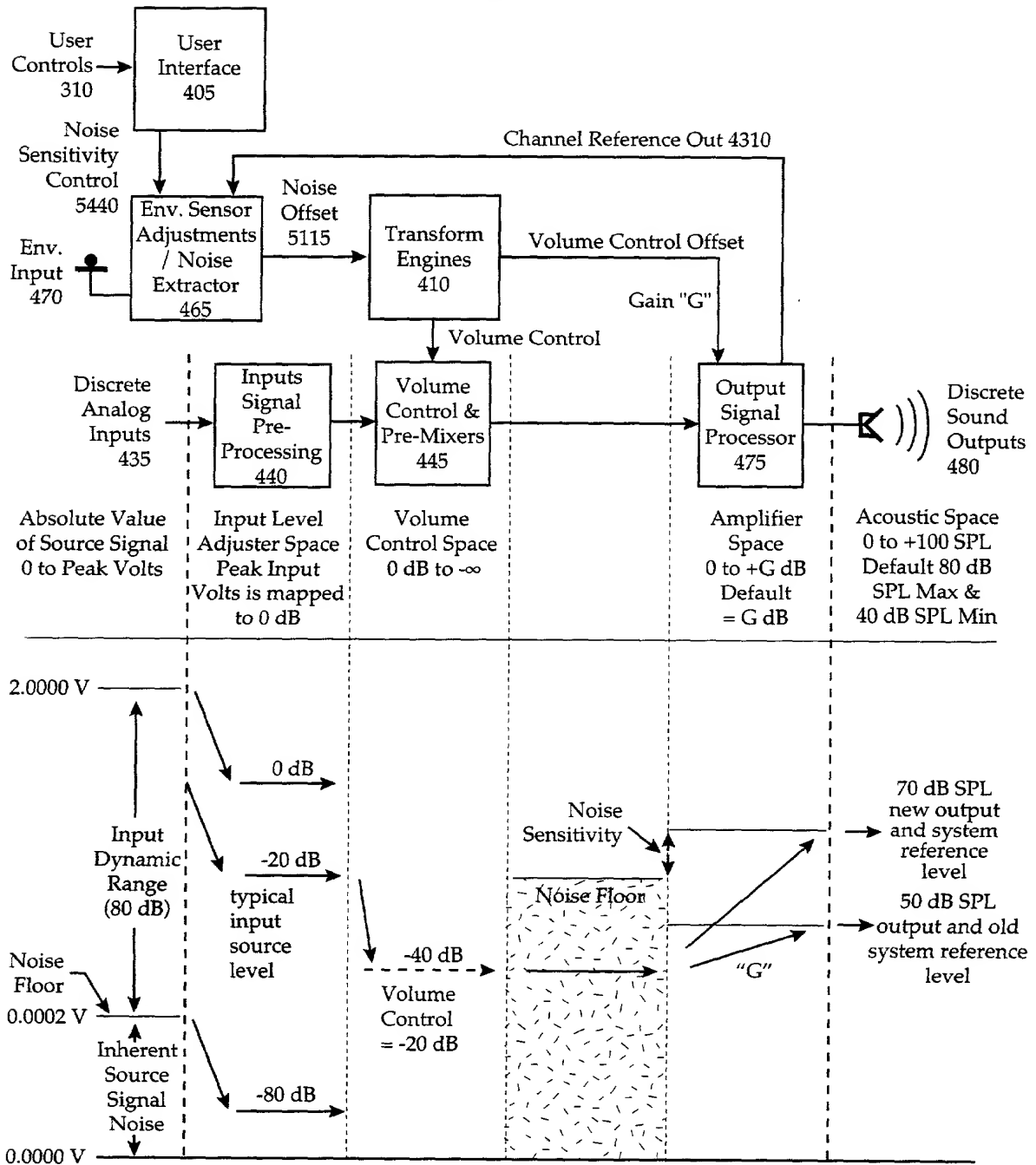


FIG. 76

Setup Command Decoder
and Setup Command Execute
660E and 660F

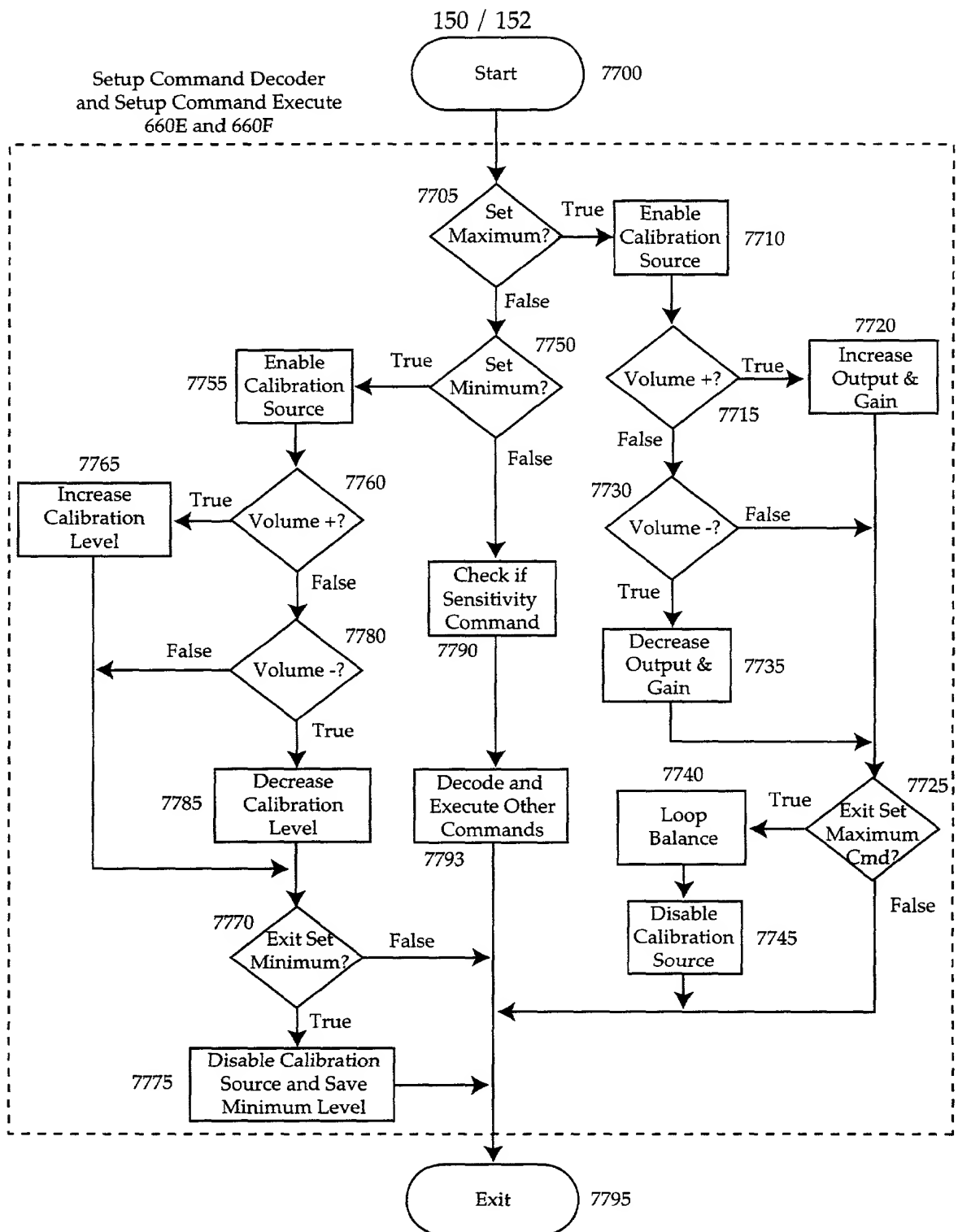
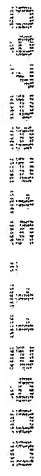


FIG. 77



7

Operation Command Decoder
and Operation Code Execute
660C and 660D

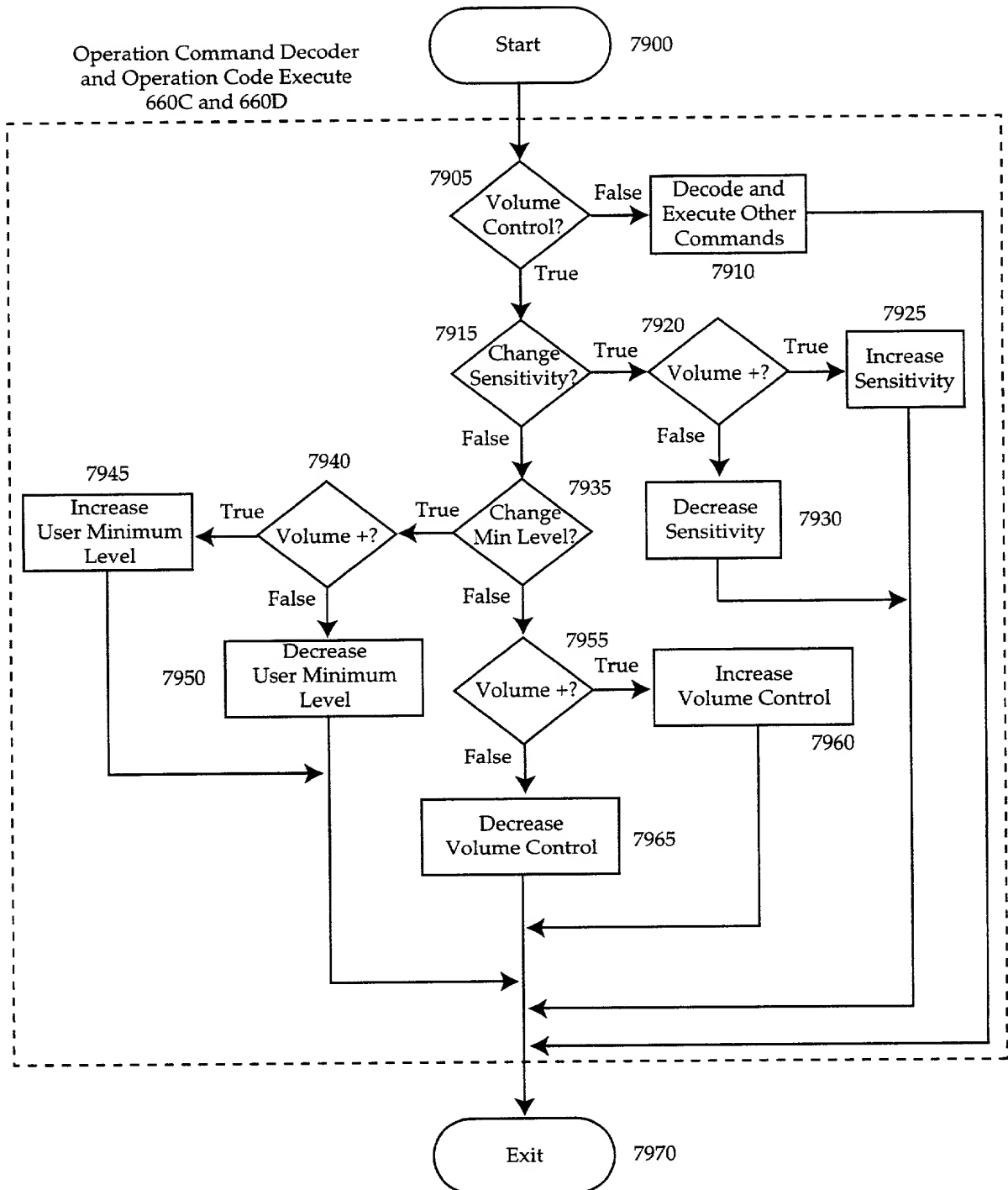


FIG. 79